Nixel 512 Datasheet

512 Electrode Neural Recording ASIC

Product Datasheet (Version 1.01)

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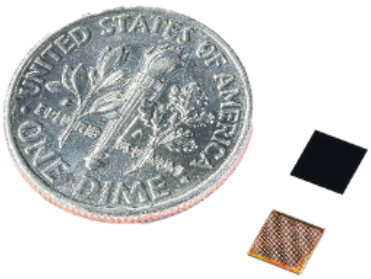


Summary

The Nixel 512™ chip is a low-noise and low-power mixed-signal programmable neural recording ASIC with 512 electrodes and 16-bit data path. It has an array of 256 differential record channels with integrated low-noise amplifiers (LNAs) and analog-to-digital converters (ADCs) that can record 512 electrodes in parallel at sampling rates up to 32 kHz with ADC resolutions up to 16-bit. The chip has a uniform array of 256 fully differential identical active neural recording elements, called nixels, acting as electrical pixels for neural recording applications. The Nixel 512 chip has a tiny chip-scale package measuring 4 mm x 4 mm, suitable for ultra compact head stages and high-density multi electrode-array (MEA) neural recording applications.

Key Features

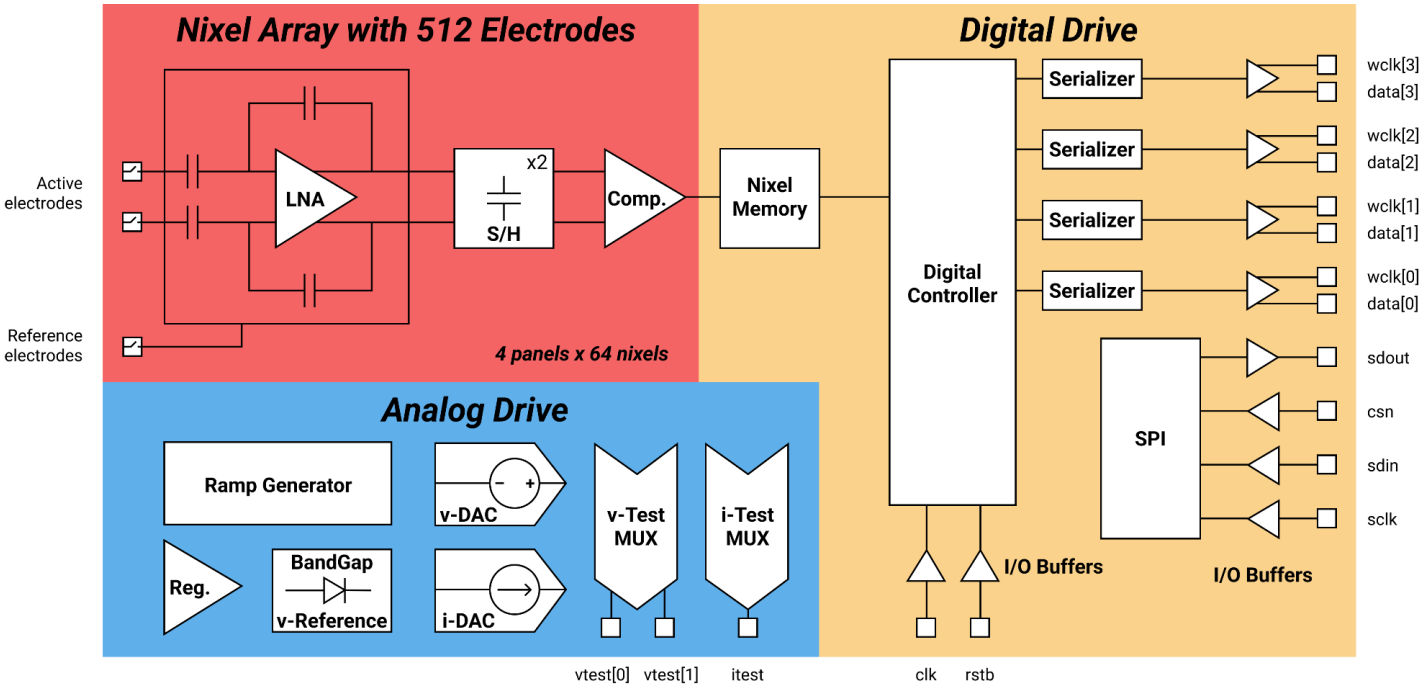
- 512 recording electrodes in a uniform array.
- 256 fully differential neural recording elements (nixels).
- User-selectable analog polarity for input and reference electrode selections.
- AC coupled LNA with in-nixel digitization with digital readout.
- Programmable nixel gain and bandwidth (BW) selection for low noise
- Input referred noise below 5 μV rms in the high gain mode
- High- and low-gain modes for spike and local field potentials (LFP) recording.
- User-selectable reference generation and distribution.
- Simultaneous spike and LFP recording up to 32 kHz sampling rate.
- Programmable ADC resolution up to 16-bit.
- Integrated impedance measurement circuit for every electrode.
- Low-power and low-voltage design (1.2 V digital and 2.5 V analog).
- Ultra small chip-scale package (4 mm x 4 mm) with Cu bumps.

Applications

- Chip-scale ultra-compact neural recording solutions for high-density MEAs.
- Ultra-compact high-density head stages with digital control and readout.
- Active MEAs for “Smart-Dish” type in vitro neural recording applications.
- Chip-scale MEAs for “Neurons-on-Chip” type neural recording applications.
- Low-noise multi-channel scientific data acquisition systems.

Architecture

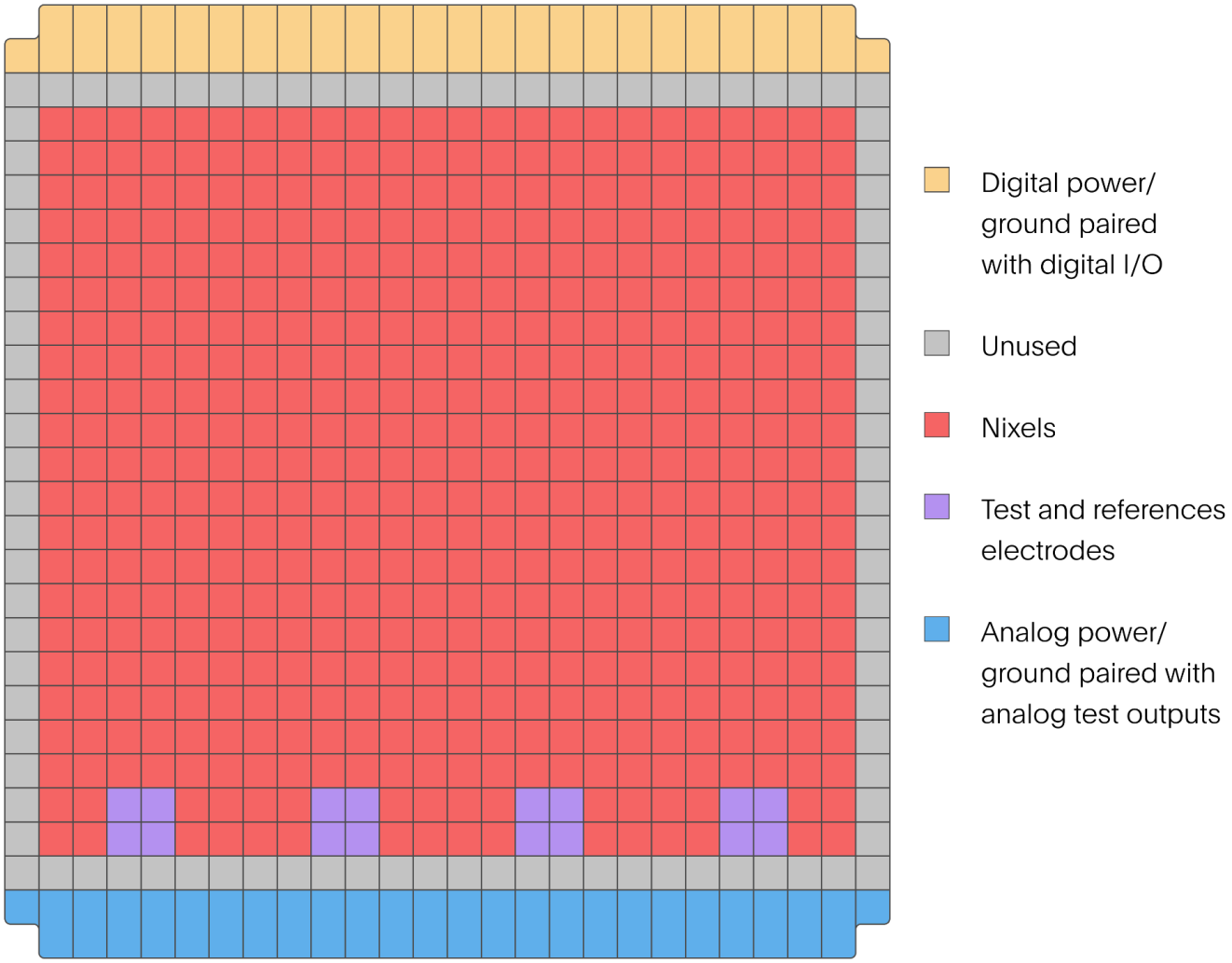
The Nixel 512™ chip is composed of the Nixel Array, Analog Drive, and Digital Drive.



The Nixel Array

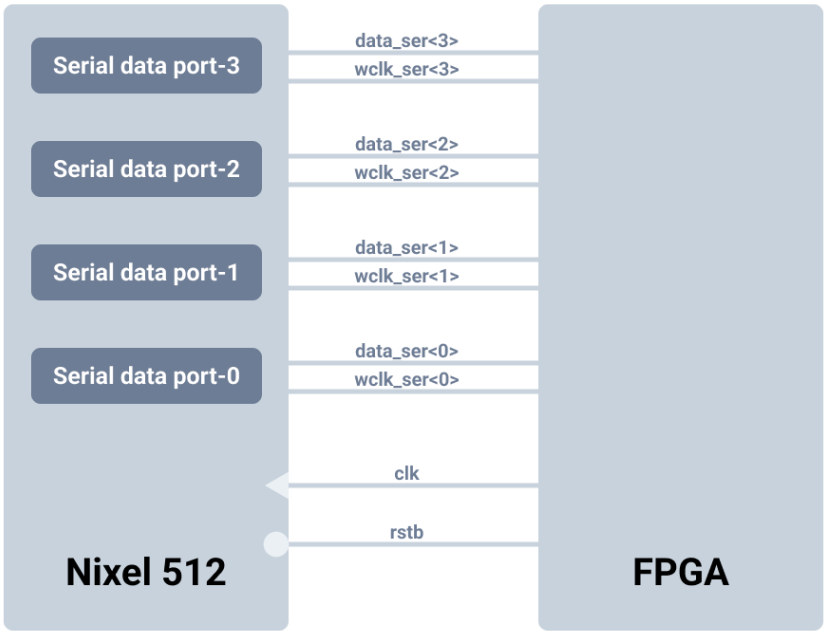
The Nixel Array is a 2D array of 256 neural recording elements, called nixels, which can each record from two electrodes simultaneously. The nixels are arranged in four identical panels, with each panel containing 128 active electrodes and 4 reference electrodes. All four panels can operate in parallel to record from all 512 electrodes at once. Every nixel has an input switch matrix, a capacitively coupled fully-differential low-noise amplifier (LNA), an analog sample and hold (S/H) circuit, and an analog comparator.

The Analog Drive generates the required currents and voltages, as well as the static and dynamic reference and test signals used by the Nixel 512 chip. The Digital Drive generates all the control and timing signals used to configure and operate the chip using a 4-wire serial programming interface (SPI).



Electrical Interface

The Nixel 512™ chip runs on dual supply voltages of 1.2 V for digital blocks and 2.5 V for analog blocks. It uses 16-bit digital data paths internally and has four serial data ports with a 16:1 serialization ratio to send out the digital recording results. Each port has a dedicated word clock to indicate the word boundaries in the serial data stream.



The Nixel 512 chip has five digital inputs and twelve digital outputs (I/Os) connected to the world using 1.2 V CMOS I/O buffers and powered with the 1.2 V digital supply of the chip. The chip also has 3-bit general purpose data outputs (GPOs) that can be controlled over SPI if needed.

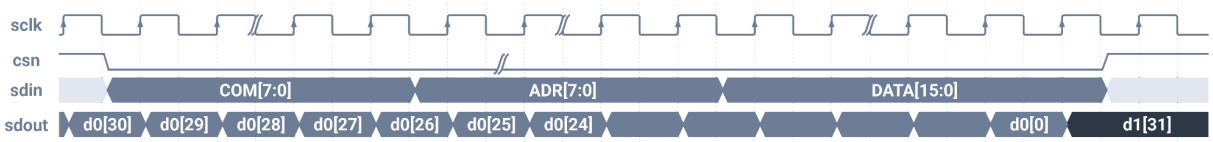
Digital I/Os

No.	I/O Name		Type	Specification
1	System	rstb	1.2V CMOS Input	Active low asynchronous reset
2		clk		System clock, ≤ 160MHz, 50% duty cycle
3	4-wire SPI	csn		Active low chip select input for SPI
4		sdin		Serial data input for SPI
5		sclk		Serial clock for SPI, sclk freq = ¼ of clk
6		sdout	1.2V CMOS Output	Serial data output of SPI
7–10	Serial data ports	data_ser_out<3:0>		Serial data port for digitized nixels
11–14		wclk_ser_out<3:0>		Word clock for serial data port
15–17	Test / GPO	digtest_out<3:0>		Digital test outputs, can be hooked to SPI

The Nixel 512 chip uses a standard 4-wire SPI interface to program and control the chip, with active low chip select (csn), serial data input (sdin), serial clock (sclk), and serial data output (sdout). SPI interface uses 32-bit words, composed of an 8-bit command (<31:24>), an 8-bit address (<23:16>), and an 16-bit

data (<15:0>) and sends the most-significant-bit (MSB) first. Since SPI operates at the rising edge of sclk, csn and sdin are applied at the falling edge of the sclk. Likewise, sdout from the SPI will be updated at the rising edge of the sclk, therefore it should be captured by the external electronics at the falling edge of sclk.

SPI timing takes 32 sclk cycles to enter the 32-bit SPI words into the input shift register of the SPI when csn is LOW. When csn is HIGH, it takes an additional 16 sclk cycles for the SPI controller to decode the SPI commands and read or write to the SPI registers. Including this idle time, an SPI operation will take 48 sclk cycles to complete. It is suggested to generate sclk from clk with a clock division ratio of 4.



The Nixel 512 chip supports clk frequencies up to 160 MHz, providing ADC sampling rates up to 12-bit resolution at 32 kHz sampling rate. In this case, ADC sampling time will be 31.25 µs, and the serial data stream for full resolution (64 nixels or 128 electrodes per panel) will only take 6.4 µs, which is less than 21% of the available ADC sampling time. In cases where 10-bit ADC resolution will be enough, a 40 MHz clk will be sufficient for the same 32 kHz ADC sampling. In this 32 kHz 10-bit ADC mode, serial data can be transmitted in 25.6 µs, which will correspond to about 82% of the available ADC sampling time. At clock frequencies less than ~33MHz, it will not be possible to maintain 32kHZ ADC sampling rate without decreasing the ADC resolution below 10-bit. If lower resolution is not an option, then the ADC sampling rate can be reduced to 16kHz or below to allow enough clock cycles for the single-slope type ADCs to perform ADC conversion. For example, 16 kHz ADC sampling with 10-bit resolution will be possible with clock frequencies just above 17 MHz.

Summary Table

<table>
<tr><td rowspan="10">Power supplies and returns (grounds)</td><td colspan="2" rowspan="3">Analog power</td><td>vdda_bg</td><td>Bias generator supply</td><td rowspan="3">2.5 V</td></tr>
<tr><td>vdda_lna</td><td>Nixel LNA supply</td></tr>
<tr><td>vdda_cmp</td><td>Nixel comparator supply</td></tr>
<tr><td colspan="2" rowspan="4">Analog ground</td><td>vssa_bg</td><td>Bias generator ground</td><td rowspan="4">0.0 V</td></tr>
<tr><td>vssa_lna</td><td>Nixel LNA ground</td></tr>
<tr><td>vssa_cmp</td><td>Nixel comparator ground</td></tr>
<tr><td>sub</td><td>Substrate, ground</td></tr>
<tr><td colspan="2" rowspan="2">Digital power</td><td>dvdd2p5</td><td>Level shifter supply</td><td>2.5 V</td></tr>
<tr><td>dvdd</td><td>Core and I/O supply</td><td>1.2 V</td></tr>
<tr><td colspan="2">Digital ground</td><td>dvss</td><td>All digital block, ground</td><td>0.0 V</td></tr>
<tr><td rowspan="4">Power dissipation</td><td rowspan="3">32 KHz sampling
12-bit ADC resolution
160 MHz clk</td><td>Analog</td><td colspan="3">≤ 22mW</td></tr>
<tr><td>Digital</td><td colspan="3">≤ 8mW</td></tr>
<tr><td>Total</td><td colspan="3">≤ 30mW</td></tr>
<tr><td colspan="4">Power dissipation can be reduced to 15 mW at 16 kHz sampling with 10-bit ADC resolution with a 20 MHz clk</td></tr>
<tr><td rowspan="12">Digital I/Os</td><td colspan="2">1.2V CMOS I/Os</td><td colspan="3">Output impedance (fixed drive strength) ≤ 100 W</td></tr>
<tr><td colspan="2" rowspan="3">Outputs</td><td colspan="3">Capacitive only loads</td></tr>
<tr><td colspan="2">High-speed data / test</td><td>SPI output</td></tr>
<tr><td colspan="2">≤ 10 pF, up to 160 MHz</td><td>≤ 40 pF, up to 40 MHz</td></tr>
<tr><td colspan="2">System inputs</td><td colspan="3">rstb: active low reset input
clk: system clock, 50% duty cycle, 160 MHz
Rise-time = fall-time ≤ 25% of clk period, 1.56ns</td></tr>
<tr><td colspan="2">4-wire SPI</td><td colspan="3">csn: active low chip select, generated at falling sclk
sdin: serial data input, generated at falling sclk
sclk: serial clk (40 MHz, 1/4th of clk frequency)
(Rise-time = fall-time ≤ 6.25 ns)
sdout: serial data output, sampled at falling sclk
(Load for sdout ≤ 40 pF)</td></tr>
<tr><td colspan="2" rowspan="5">Serial data ports</td><td colspan="3">160 Mbps at 160 MHz system clock
Load for data ports ≤ 10 pF</td></tr>
<tr><td>Port-0</td><td colspan="2">data_ser_out<0>
wclk_ser_out<0></td></tr>
<tr><td>Port-1</td><td colspan="2">data_ser_out<1>
wclk_ser_out<1></td></tr>
<tr><td>Port-2</td><td colspan="2">data_ser_out<2>
wclk_ser_out<2></td></tr>
<tr><td>Port-3</td><td colspan="2">data_ser_out<3>
wclk_ser_out<3></td></tr>
<tr><td rowspan="4">Package</td><td colspan="2">Flip-chip CSP with Cu bumps</td><td colspan="3">4 mm x 4 mm</td></tr>
<tr><td colspan="2">Bump array / pitch</td><td>28 x 26</td><td>724 Bumps (none on corners)</td><td>140 µm</td></tr>
<tr><td colspan="2">Cu bump composition</td><td colspan="3">40 µm Cu + 20 µm SnAg</td></tr>
<tr><td colspan="2">Die thickness</td><td colspan="3">12 mil (~305 µm)</td></tr>
</table>

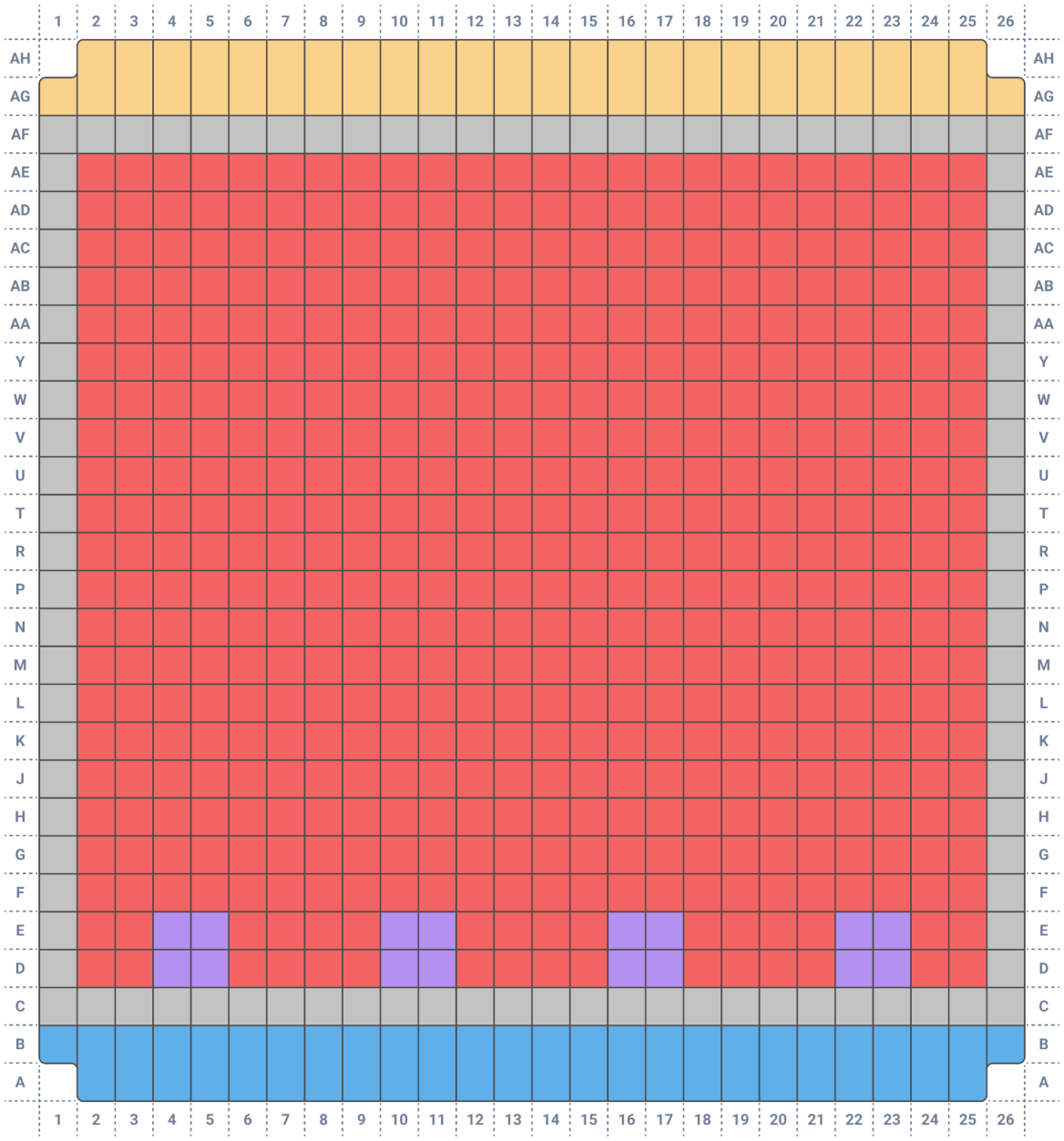
Technical Table

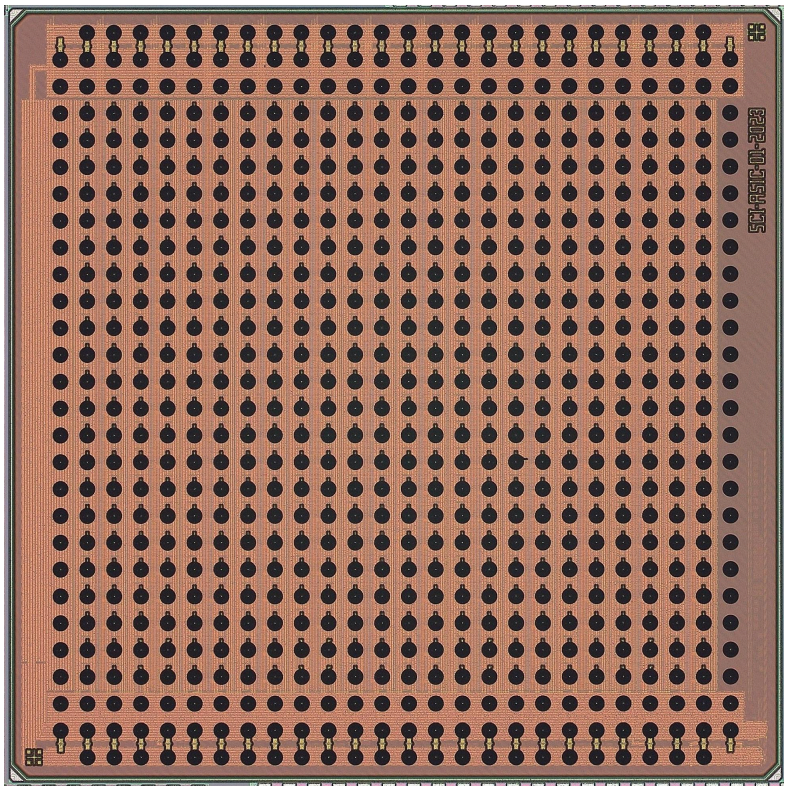
Active electrodes	Active	Reference	Test	
	512	8	8	
Input capacitance	6.8 pF			
Panel count	4 panels			
	One panel has 128 active electrodes, 2 reference, and 2 test electrodes			
Neural interface elements (nixels)	Selectable input configuration			
	Differential or single-ended operation			
	LNA + S/H + Comparator			
LNA parameters	Parameter name	Min	Max	
	Gain, input referred noise	13 V/V, 27 µV rms	200 V/V, 4.5 µV rms	
	High-pass corner	3.8 Hz	460 Hz	
	Low-pass corner	1.45 kHz	14 kHz	
Sample-and-hold (S/H)	Ping-pong architecture, with dual analog memory			
Comparator	In-nixel digitization with comparator Analog front-end of single-slope ADC			
ADC parameters	Single-slope-ADC, distributed architecture			
	User selectable resolution, 12–16-bit in resolution, ≤ 32 kHz in sampling			
	ADC Mode-0: *Low resolution, high sample rate*	10-bit @ 32 kHz sampling, 40 MHz clk		
	ADC Mode-1: *High resolution, mid sample rate*	12-bit @ 16 kHz sampling, 80 MHz clk		
	ADC Mode-2: *High resolution, high sample rate*	12-bit @ 32 kHz sampling, 160 MHz clk		
	ADC Mode-3: *Very high resolution low sample rate*	14-bit @ 8 kHz sampling, 160 MHz clk		
	ADC Mode-4: *Ultra high resolution very low sample rate*	16-bit @ 2kHz sampling, 160 MHz clk		
Active electrodes	Configurations	Total	Spike	LFP
	Differential, all for spike	512	480	32
	Diff. spike, single ended LFP	496	480	16
	Single ended spike, single ended LFP	256	240	16
Reference electrodes	2 external reference electrodes / panel	Spike and LFP nixels have separate external reference electrode connections		
	2 external reference electrodes / chip			
	1 external reference electrodes / panel	Single external reference electrode		
	Programmable internal reference	Using internal DACs as reference		
Analog drive	On-chip bias generation	Band-gap based programmable bias generation using voltage and current mode DACs		
		12-bit v-DACs (references and test signals)		
		7-bit i-DACs		
	Ramp generation for ADC	Programmable ramp generation for ADC with variable slope and reset parameters		
Digital drive	Flexible and programmable operation of the chip	Programmable static circuit configuration of analog and digital circuits in terms of connectivity		

		Programmable timing generation for nixels and ADCs to adjust resolution and conversion time
		Command based operation of the chip
		Address based programming over SPI
Programming interface	Serial	4-wire SPI
		32-bit SPI Words
		8-bit command, 8-bit address, 16-bit data
		“48 sclk cyles” per SPI operation
Test outputs	Analog	2 Analog voltage test output pads to monitor on-chip generated biases and reference voltages using a pseudo-differential way
		Voltage test outputs can be used to overwrite internally generated biases and references, including the global routing resources for reference and test electrodes used in the Nixel Array
		1 test current output to monitor on-chip generated reference and i-DAC output current
	Digital	3-bit digital test outputs to monitor internal digital signals can also be configured to work as general-purpose output pins controlled over SPI

Packaging

The Nixel 512™ chip measures 4 mm x 4 mm x 0.3 mm and uses chip scale packaging with Cu bumps. The 2D bump array counts 28 rows and 26 columns with 724 total bumps (no bumps on corners) and a uniform bump pitch of 140 µm.

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Bump Locations

Nixel 512 Chip				Center of Bump			I/O Type	Explanation	Value	Comment	Regulators	Direction	Avg. Current, Range, Resolution
Rows		Col	Bump Name	X (um)	Y0 (um)	Y1 (um)							
A	B	1	sub	240	100	240	Analog power / ground	Substrate	0.0 V				
		2	vssa_bg	380				Ground / analog / bandgap	0.0 V				
		3	vdda_bg	520				Supply / analog / bandgap	2.5 V	1.8–2.8 V adjustable	REG-1	SOURCE	≤ 5 mA (DC)
		4	vdda_lna	660				Supply / analog / LNA	2.5 V		REG-2	SOURCE	≤ 10 mA (close to DC)
		5	vssa_lna	800				Ground / analog / LNA	0.0 V				
		6	vssa_cmp	940				Ground /analog / comparator	0.0 V				
		7	vdda_cmp	1080				Supply / analog / comparator	2.5 V		REG-3	SOURCE	≤10mA (close to DC)
		8	dvdd2p5	1220				Supply / 2.5 V digital Blocks	2.5 V		REG-4	SOURCE	≤5mA (switching)
		9	dvdd	1360				Supply / digital / core + IOs	1.2 V		REG-5	SOURCE	≤ 5mA (switching)
		10	dvss	1500				Ground / digital / core + IOs	0.0 V				
		11	sub	1640				Substrate	0.0 V				

Nixel 512 Chip				Center of Bump			I/O Type	Explanation	Value	Comment	Regulators	Direction	Avg. Current, Range, Resolution
Rows		Col	Bump Name	X (um)	Y0 (um)	Y1 (um)							
A	B	12	vdda_lna	1780	100	240	Analog power / ground	Supply / analog / LNA	2.5 V				
		13	vssa_lna	1920				Ground / analog / LNA	0.0 V				
		14	vssa_cmp	2060				Ground /analog / comparator	0.0 V				
		15	vdda_cmp	2200				Supply / analog / comparator	2.5 V				
		16	dvdd2p5	2340				Supply / 2.5V digital blocks	2.5 V				
		17	dvdd	2480				Supply / digital / core + IOs	1.2 V				
		18	dvss	2620				Ground / digital / core + IOs	0.0 V				
		19	sub	2760				Substrate	0.0 V				
		20	vdda_lna	2900				Supply / analog / LNA	2.5 V				
		21	vssa_lna	3040				Ground / analog / LNA	0.0 V				
		22	vssa_cmp	3180				Ground /analog / comparator	0.0 V				
		23	vdda_cmp	3320				Supply / analog / comparator	2.5 V				

Nixel 512 Chip				Center of Bump			I/O Type	Explanation	Value	Comment	Regulators	Direction	Avg. Current, Range, Resolution
Rows		Col	Bump Name	X (um)	Y0 (um)	Y1 (um)							
A	B	24	itest_out	3460	100	240	Analog power / ground	Current test pad / analog / bias generator	0–32 µA sourcing (p-mirror)				
		25	vtest_out <0>	3600				Voltage test pad [0] / analog / bias generator	0–2.5 V v-DAC outputs				
		26	vtest_out <1>	3740				Voltage test pad [1] / analog / bias generator	0–2.5 V v-DAC outputs				
AG	AH	1	sub	240	3740	3880	Digital power / ground / IOs	Substrate	0.0 V				
		2	dvss	380				Ground / digital / core + IOs	0.0 V				
		3	dvdd	520				Supply / digital / core + IOs	1.2 V				
		4	csn	660				CMOS (1.2) input: SPI chip select bar	0–1.2 V	From FPGA, at negedge sclk, 50 Ω series res			
		5	sdin	800				CMOS (1.2) input: SPI data in	0–1.2V	From FPGA, at negedge sclk, 50 Ω series res			

Nixel 512 Chip				Center of Bump			I/O Type	Explanation	Value	Comment	Regulators	Direction	Avg. Current, Range, Resolution
Rows		Col	Bump Name	X (um)	Y0 (um)	Y1 (um)							
AG	AH	6	sclk	940	3740	3880	Digital power / ground / IOs	CMOS (1.2) input: SPI clock	0–1.2 V, fsclk = 1/4 fclk, ≤ 40 MHz, 50% DTC	From FPGA, at negedge sclk, 50 Ω series res			
		7	sdout	1080				CMOS (1.2) output: SPI data out	0 - 1.2 V	To FPGA, at posedge sclk, 50 Ω series res			
		8	rstb	1220				Active low asynch. reset	0 - 1.2 V	From FPGA, 50 or 20 Ω series res			
		9	clk	1360				Clock	0 - 1.2V, fclk ≤ 160 MHz, 50% DTC	From FPGA, 50 or 20 Ω series res			
		10	sub	1500				Substrate	0.0 V				
		11	dvss	1640				Ground / digital / core + IOs	0.0 V				
		12	dvdd	1780				Supply / digital / core + IOs	1.2 V				
		13	data_ser <0>	1920				CMOS (1.2) output: serializer data output [0]	SDR data rate, at rising edge clk, ≤ 160 Mbps	To FPGA, 50 or 20 Ω series res			

Nixel 512 Chip				Center of Bump			I/O Type	Explanation	Value	Comment	Regulators	Direction	Avg. Current, Range, Resolution
Rows		Col	Bump Name	X (um)	Y0 (um)	Y1 (um)							
AG	AH	14	wclk_ser <0>	2060	3740	3880	Digital power / ground / IOs	CMOS (1.2) output: serializer word clock output [0]	Frequency = 1/16 of SDR data rate	To FPGA, 50 or 20 Ω series res			
		15	data_ser <1>	2200				CMOS (1.2) output: serializer data output [1]	SDR data rate, at rising edge clk, ≤ 160 Mbps	To FPGA, 50 or 20 Ω series res			
		16	wclk_ser <1>	2340				CMOS (1.2) output: serializer word clock output [1]	Frequency = 1/16 of SDR data rate	To FPGA, 50 or 20 Ω series res			
		17	data_ser <2>	2480				CMOS (1.2) output: serializer data output [2]	SDR data rate, at rising edge clk, ≤ 160 Mbps	To FPGA, 50 or 20 Ω series res			
		18	wclk_ser <2>	2620				CMOS (1.2) output: serializer word clock output [2]	Frequency = 1/16 of SDR data rate	To FPGA, 50 or 20 Ω series res			
		19	data_ser <3>	2760				CMOS (1.2) output: serializer data output [3]	SDR data rate, at rising edge clk, ≤ 160 Mbps	To FPGA, 50 or 20 Ω series res			

Nixel 512 Chip				Center of Bump			I/O Type	Explanation	Value	Comment	Regulators	Direction	Avg. Current, Range, Resolution
Rows		Col	Bump Name	X (um)	Y0 (um)	Y1 (um)							
AG	AH	20	wclk_ser <3>	2900	3740	3880	Digital power / ground / IOs	CMOS (1.2) output: serializer word clock output [3]	Frequency = 1/16 of SDR data rate	To FPGA, 50 or 20 Ω series res			
		21	sub	3040				Substrate	0.0 V				
		22	dvss	3180				Ground / digital / core + IOs	0.0 V				
		23	dvdd	3320				Supply / digital / Core + IOs	1.2 V				
		24	digtest <0>	3460				CMOS (1.2) digital test output [0]	0–1.2 V	To FPGA, 50 or 20 Ω series res			
		25	digtest <1>	3600				CMOS (1.2) digital test output [1]	0–1.2 V	To FPGA, 50 or 20 Ω series res			
		26	digtest <2>	3740				CMOS (1.2) digital test output [2]	0–1.2 V	To FPGA, 50 or 20 Ω series res			

Contact Information

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