Nixel 512 Datasheet

512 Electrode Neural Recording ASIC

Product Datasheet (Version 1.1)

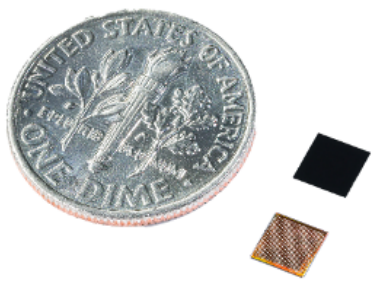
Science Corporation
300 Wind River Way, Alameda, CA 94501

www.science.xyz/technologies/chips/nixel-512

Table of Contents

Summary

The Nixel 512™ chip is a low-noise and low-power mixed-signal programmable neural recording ASIC with 512 electrodes and 16-bit data path. It has an array of 256 differential record channels with integrated low-noise amplifiers (LNAs) and analog-to-digital converters (ADCs) that can record 512 electrodes in parallel at sampling rates up to 32 kHz with ADC resolutions up to 16-bit. The chip has a uniform array of 256 fully differential identical active neural recording elements, called nixels, acting as electrical pixels for neural recording applications. The Nixel 512 chip has a tiny chip-scale package measuring 4 mm x 4 mm, suitable for ultra compact head stages and high-density multi electrode-array (MEA) neural recording applications.



Key Features

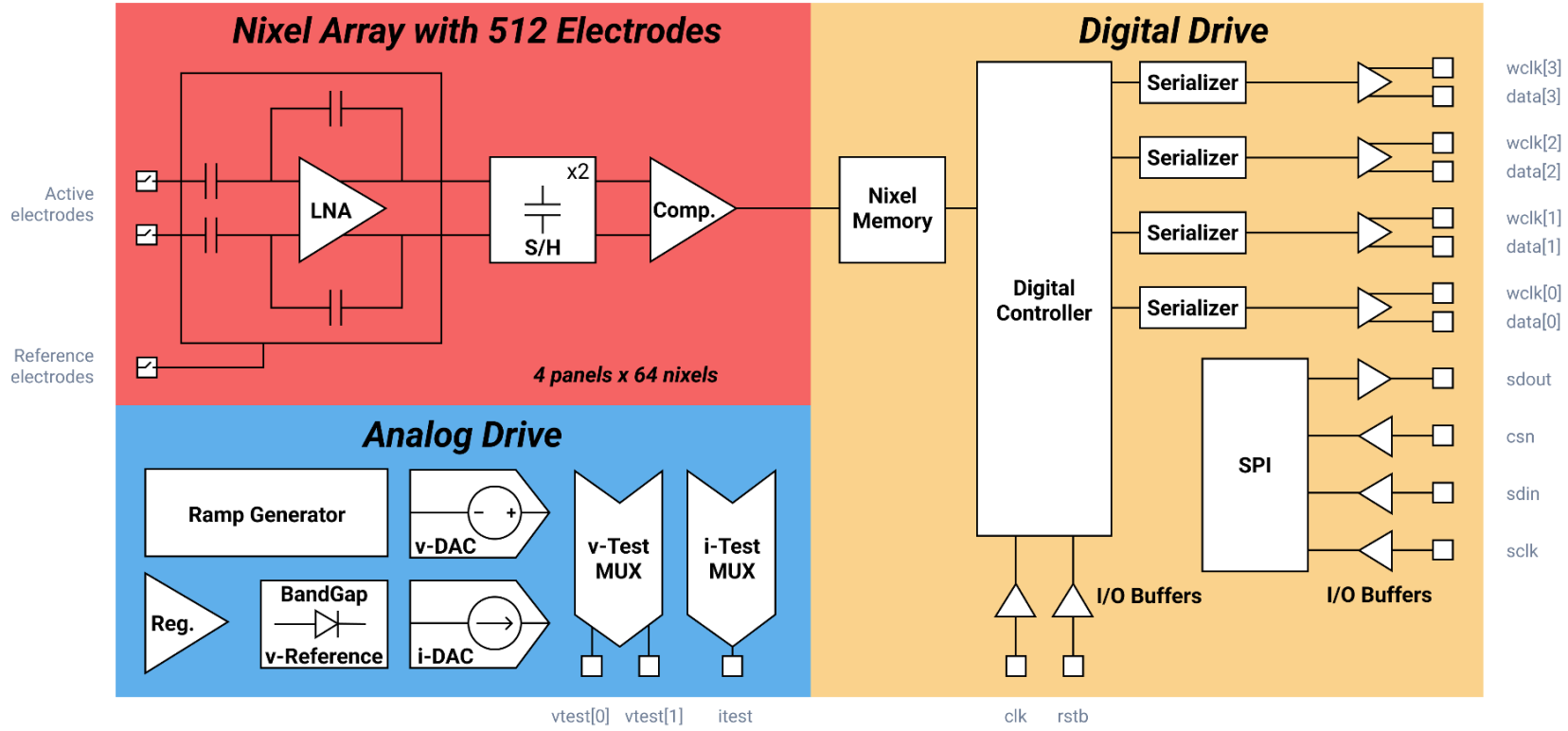
- 512 recording electrodes in a uniform array.
- 256 fully differential neural recording elements (nixels).
- User-selectable analog polarity for input and reference electrode selections.
- AC coupled LNA with in-nixel digitization with digital readout.
- Programmable nixel gain and bandwidth (BW) selection for low noise.
- Input referred noise below 5 µV rms in the high gain mode.
- High- and low-gain modes for spike and local field potentials (LFP) recording.
- User-selectable reference generation and distribution.
- Simultaneous spike and LFP recording up to 32 kHz sampling rate.
- Programmable ADC resolution from 10 to 16-bit.
- Integrated impedance measurement for all 512 electrodes.
- Low-power and low-voltage design (1.2 V digital and 2.5 V analog).
- Wafer level chip-scale package (WLCSP): 4 mm x 4 mm (Cu bumps).

Applications

- Chip-scale ultra-compact neural recording solutions for high-density MEAs.
- Ultra-compact high-density head stages with digital control and readout.
- Active MEAs for “Smart-Dish” type in vitro neural recording applications.
- Chip-scale MEAs for “Neurons-on-Chip” type neural recording applications.
- Low-noise multi-channel scientific data acquisition systems.

Architecture

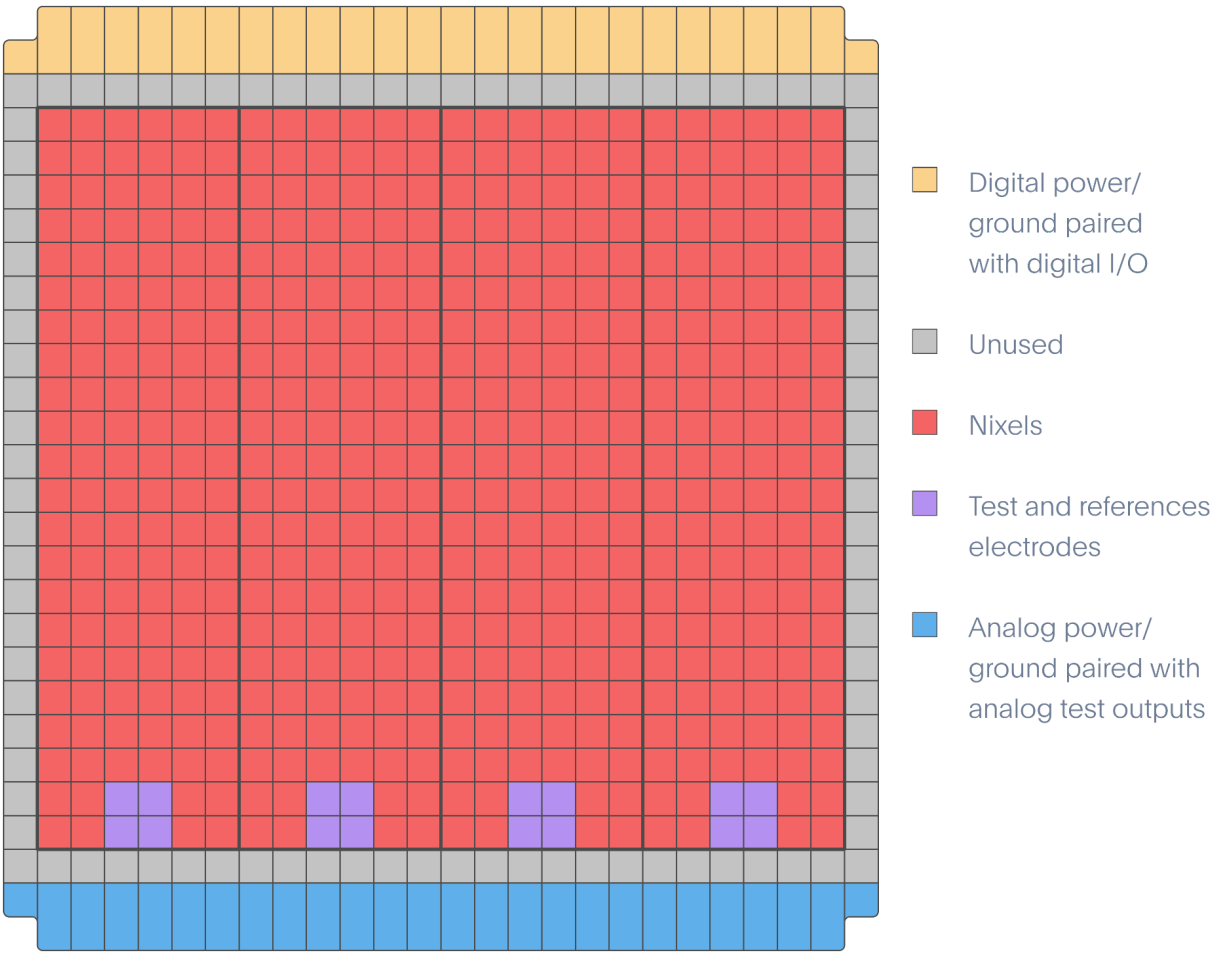
The Nixel 512 chip is composed of the Nixel Array, Analog Drive, and Digital Drive.



The Nixel Array

The Nixel Array is a 2D array of 256 neural recording elements, called nixels, which can each record from two electrodes simultaneously. Every nixel has an input switch matrix, a capacitively coupled fully-differential low-noise amplifier (LNA), an analog sample and hold (S/H) circuit, and an analog comparator.

The Analog Drive generates the required currents and voltages, as well as the static and dynamic reference and test signals used by the Nixel 512 chip. The Digital Drive generates all the control and timing signals used to configure and operate the chip using a 4-wire serial programming interface (SPI).



Electrode Input Arrangement

The nixels are arranged in four identical panels, with each panel containing 128 electrode inputs. Each nixel is a differential amplifier connected to two electrode sites, labeled as even and odd.

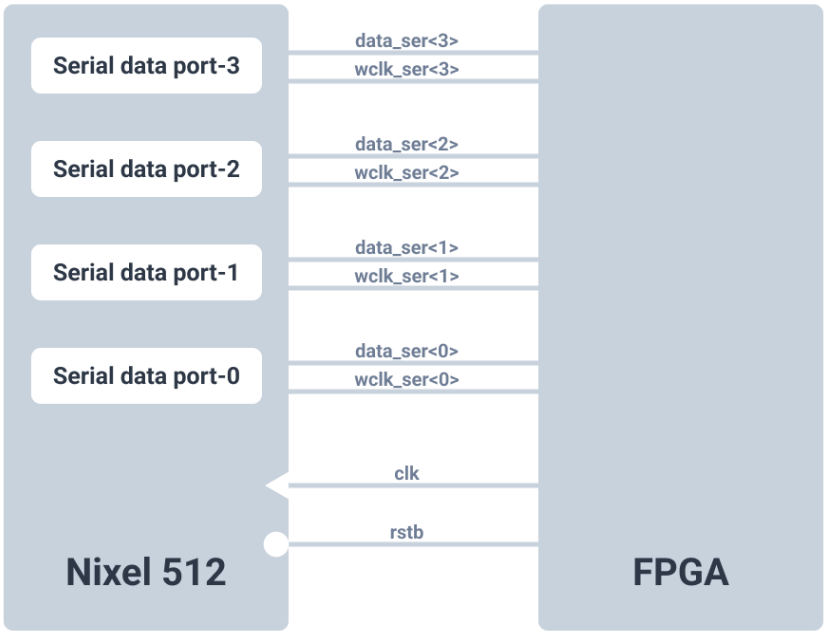
The bottom two rows of nixels contain reference and test electrode inputs. Pin R1 is the LFP nixel reference, pin R2 is the spike nixel reference, and pins T1 and T2 can be used for testing purposes. The four adjacent nixels [0–7] are used for LFP recording while nixels [8–127] are used for spike recording. You can program the LFP nixels and spike nixels to have independent input switch configurations, gain, high-pass and low-pass filter corner settings.

All four panels can operate in parallel to record from all 512 electrodes at once. For the simplest configuration, you can connect all 16 reference and test electrode inputs together to a large reference electrode located in your active area.

122	123	124	125	126	127
116	117	118	119	120	121
110	111	112	113	114	115
104	105	106	107	108	109
98	99	100	101	102	103
92	93	94	95	96	97
86	87	88	89	90	91
80	81	82	83	84	85
74	75	76	77	78	79
68	69	70	71	72	73
62	63	64	65	66	67
56	57	58	59	60	61
50	51	52	53	54	55
44	45	46	47	48	49
38	39	40	41	42	43
32	33	34	35	36	37
26	27	28	29	30	31
20	21	22	23	24	25
14	15	16	17	18	19
8	9	10	11	12	13
4	5	T1	T2	6	7
0	1	R1	R2	2	3

Electrical Interface

The Nixel 512 chip runs on dual supply voltages of 1.2 V for digital blocks and 2.5 V for analog blocks. It uses 16-bit digital data paths internally and has four serial data ports with a 16:1 serialization ratio to send out the digital recording results. Each port has a dedicated word clock to indicate the word boundaries in the serial data stream.



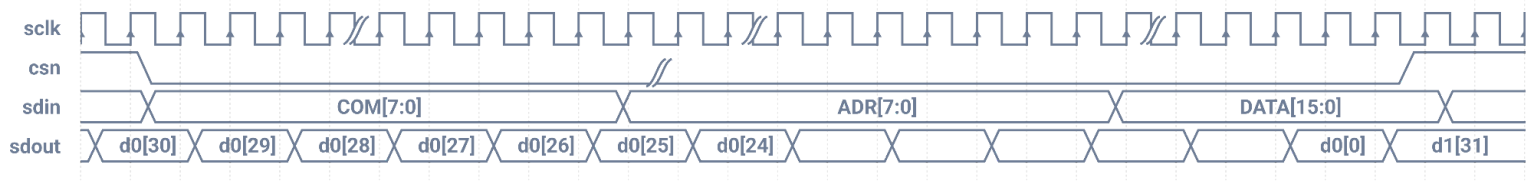
The Nixel 512 chip has five digital inputs and twelve digital outputs (I/Os) connected to the world using 1.2 V CMOS I/O buffers and powered with the 1.2 V digital supply of the chip. The chip also has 3-bit general purpose data outputs (GPOs) that can be controlled over SPI if needed.

Digital I/Os

No.	I/O Name		Type	Specification
1	System	rstb	1.2V CMOS Input	Active low asynchronous reset
2		clk		System clock, ≤ 160 MHz, 50% duty cycle
3	4-wire SPI	csn		Active low chip select input for SPI
4		sdin		Serial data input for SPI
5		sclk		Serial clock for SPI, sclk freq = ¼ of clk
6		sdout	1.2V CMOS Output	Serial data output of SPI
7–10	Serial data ports	data_ser_out<3:0>		Serial data port for digitized nixels
11–14		wclk_ser_out<3:0>		Word clock for serial data port
15–17	Test / GPO	digtest_out<3:0>		Digital test outputs, can be hooked to SPI

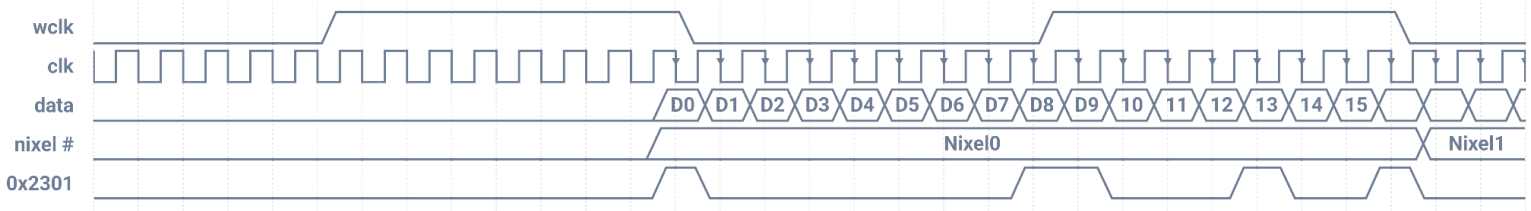
The Nixel 512 chip uses a 4-wire SPI interface to program and control the chip, with active low chip select (csn), serial data input (sdin), serial clock (sclk), and serial data output (sdout). SPI interface uses 32-bit words, composed of an 8-bit command (<31:24>), an 8-bit address (<23:16>), and an 16-bit data (<15:0>) and sends the most-significant-bit (MSB) first. Since SPI operates at the rising edge of sclk, csn and sdin

are applied at the falling edge of the sclk. Likewise, sdout from the SPI will be updated at the rising edge of the sclk, therefore it should be captured by the external electronics at the falling edge of sclk.

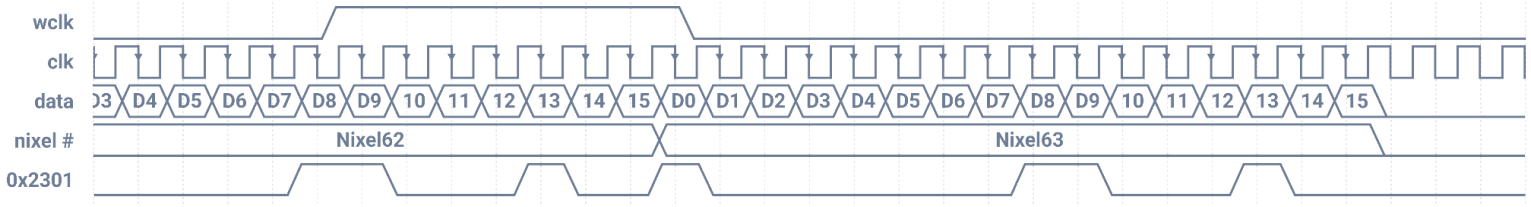


SPI timing takes 32 sclk cycles to enter the 32-bit SPI words into the input shift register of the SPI when csn is LOW. When csn is HIGH, it takes an additional 16 sclk cycles for the SPI controller to decode the SPI commands and read or write to the SPI registers. Including this idle time, an SPI operation will take 48 sclk cycles to complete. It is suggested to generate sclk from clk with a clock division ratio of 4.

Prior to streaming out a window of nixels, a panel keeps wclk and data low. For each enabled nixel in a panel (based on the window register settings), the panel will send a word. Each word is prefixed by a wclk high pulse—the corresponding 16 bits are sent out **starting when wclk goes low**—the data bits are valid on the *falling edge* of the clk:



The last wclk will appear as:



The Nixel 512 chip supports clk frequencies up to 160 MHz, providing ADC sampling rates up to 12-bit resolution at 32 kHz sampling rate. In this case, ADC sampling time will be 31.25 µs, and the serial data stream for full resolution (64 nixels or 128 electrodes per panel) will only take 6.4 µs, which is less than 21% of the available ADC sampling time. In cases where 10-bit ADC resolution will be enough, a 40 MHz clk will be sufficient for the same 32 kHz ADC sampling. In this 32 kHz 10-bit ADC mode, serial data can be transmitted in 25.6 µs, which will correspond to about 82% of the available ADC sampling time. At clock frequencies less than ~33MHz, it will not be possible to maintain 32kHZ ADC sampling rate without decreasing the ADC resolution below 10-bit. If lower resolution is not an option, then the ADC sampling rate can be reduced to 16kHz or below to allow enough clock cycles for the single-slope type ADCs to perform ADC conversion. For example, 16 kHz ADC sampling with 10-bit resolution will be possible with clock frequencies just above 17 MHz.

Summary Table

<table>
<tr><td rowspan="10">Power supplies and returns (grounds)</td><td rowspan="3">Analog power</td><td colspan="2">vdda_bg</td><td>Bias generator supply</td><td rowspan="3">2.5 V</td></tr>
<tr><td colspan="2">vdda_lna</td><td>Nixel LNA supply</td></tr>
<tr><td colspan="2">vdda_cmp</td><td>Nixel comparator supply</td></tr>
<tr><td rowspan="4">Analog ground</td><td colspan="2">vssa_bg</td><td>Bias generator ground</td><td rowspan="4">0.0 V</td></tr>
<tr><td colspan="2">vssa_lna</td><td>Nixel LNA ground</td></tr>
<tr><td colspan="2">vssa_cmp</td><td>Nixel comparator ground</td></tr>
<tr><td colspan="2">sub</td><td>Substrate, ground</td></tr>
<tr><td rowspan="2">Digital power</td><td colspan="2">dvdd2p5</td><td>Level shifter supply</td><td>2.5 V</td></tr>
<tr><td colspan="2">dvdd</td><td>Core and I/O supply</td><td>1.2 V</td></tr>
<tr><td>Digital ground</td><td colspan="2">dvss</td><td>All digital block, ground</td><td>0.0 V</td></tr>
<tr><td rowspan="4">Power dissipation</td><td rowspan="3">32 KHz sampling
12-bit ADC resolution
160 MHz clk</td><td>Analog</td><td colspan="3">≤ 22mW</td></tr>
<tr><td>Digital</td><td colspan="3">≤ 8mW</td></tr>
<tr><td>Total</td><td colspan="3">≤ 30mW</td></tr>
<tr><td colspan="5">Power dissipation can be reduced to 15 mW at 16 kHz sampling with 10-bit ADC resolution with a 20 MHz clk</td></tr>
<tr><td rowspan="11">Digital I/Os</td><td>1.2V CMOS I/Os</td><td colspan="4">Output impedance (fixed drive strength) ≤ 100 W</td></tr>
<tr><td rowspan="3">Outputs</td><td colspan="4">Capacitive only loads</td></tr>
<tr><td colspan="2">High-speed data / test</td><td colspan="2">SPI output</td></tr>
<tr><td colspan="2">≤ 10 pF, up to 160 MHz</td><td colspan="2">≤ 40 pF, up to 40 MHz</td></tr>
<tr><td colspan="2">System inputs</td><td colspan="4">rstb: active low reset input
clk: system clock, 50% duty cycle, 160 MHz
Rise-time = fall-time ≤ 25% of clk period, 1.56ns</td></tr>
<tr><td colspan="2">4-wire SPI</td><td colspan="4">csn: active low chip select, generated at falling sclk
sdin: serial data input, generated at falling sclk
sclk: serial clk (40 MHz, 1/4th of clk frequency)
(Rise-time = fall-time ≤ 6.25 ns)
sdout: serial data output, sampled at falling sclk
(Load for sdout ≤ 40 pF)</td></tr>
<tr><td rowspan="5">Serial data ports</td><td colspan="4">160 Mbps at 160 MHz system clock
Load for data ports ≤ 10 pF</td></tr>
<tr><td colspan="2">Port-0</td><td colspan="2">data_ser_out<0>
wclk_ser_out<0></td></tr>
<tr><td colspan="2">Port-1</td><td colspan="2">data_ser_out<1>
wclk_ser_out<1></td></tr>
<tr><td colspan="2">Port-2</td><td colspan="2">data_ser_out<2>
wclk_ser_out<2></td></tr>
<tr><td colspan="2">Port-3</td><td colspan="2">data_ser_out<3>
wclk_ser_out<3></td></tr>
<tr><td rowspan="4">Package</td><td colspan="2">Flip-chip CSP with Cu bumps</td><td colspan="4">4 mm x 4 mm</td></tr>
<tr><td colspan="2">Bump array / pitch</td><td>28 x 26</td><td>724 Bumps
(none on corners)</td><td>140 µm</td></tr>
<tr><td colspan="2">Cu bump composition</td><td colspan="4">40 µm Cu + 20 µm SnAg</td></tr>
<tr><td colspan="2">Die thickness</td><td colspan="4">12 mil (~305 µm)</td></tr>
</table>

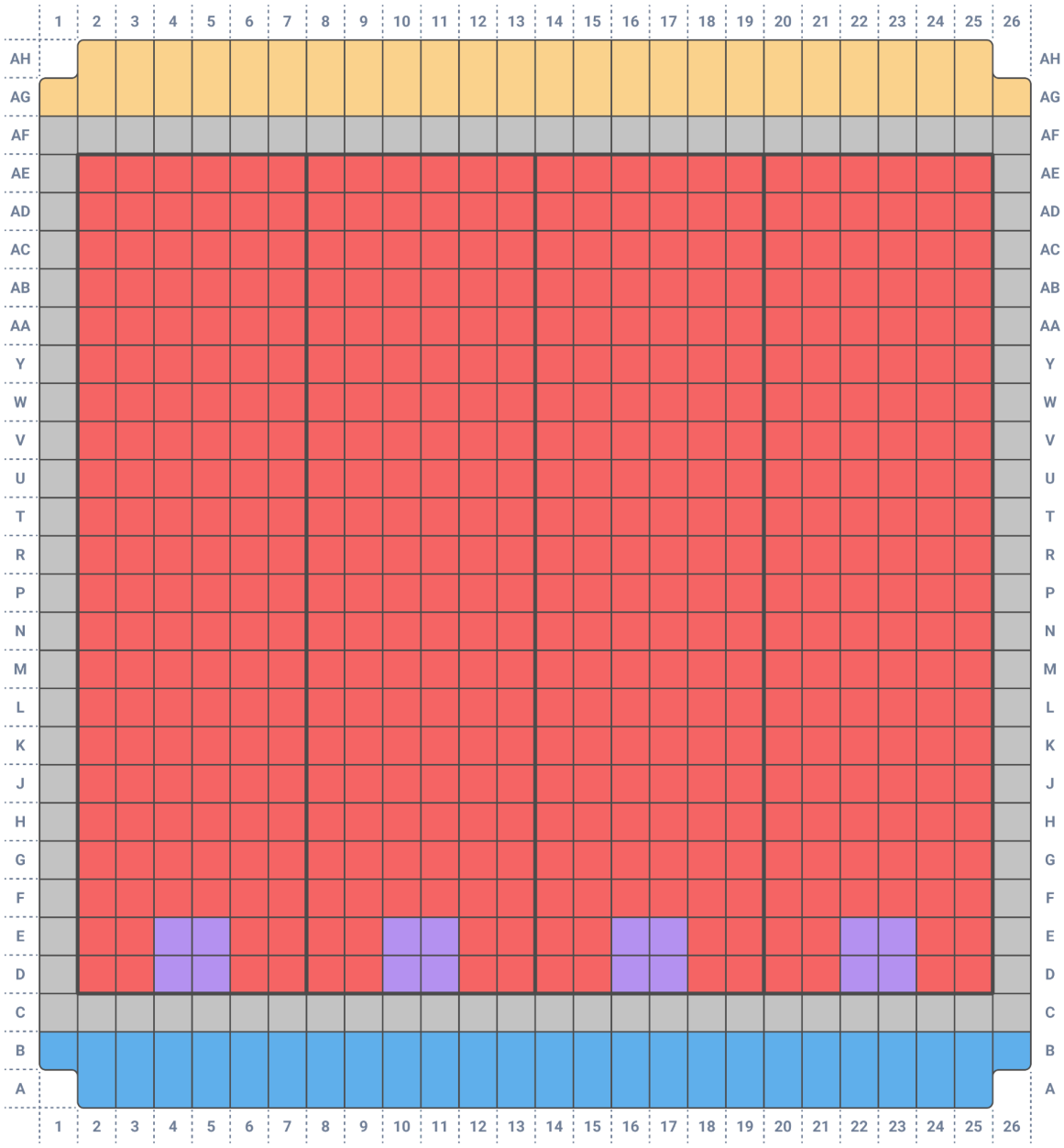
Technical Table

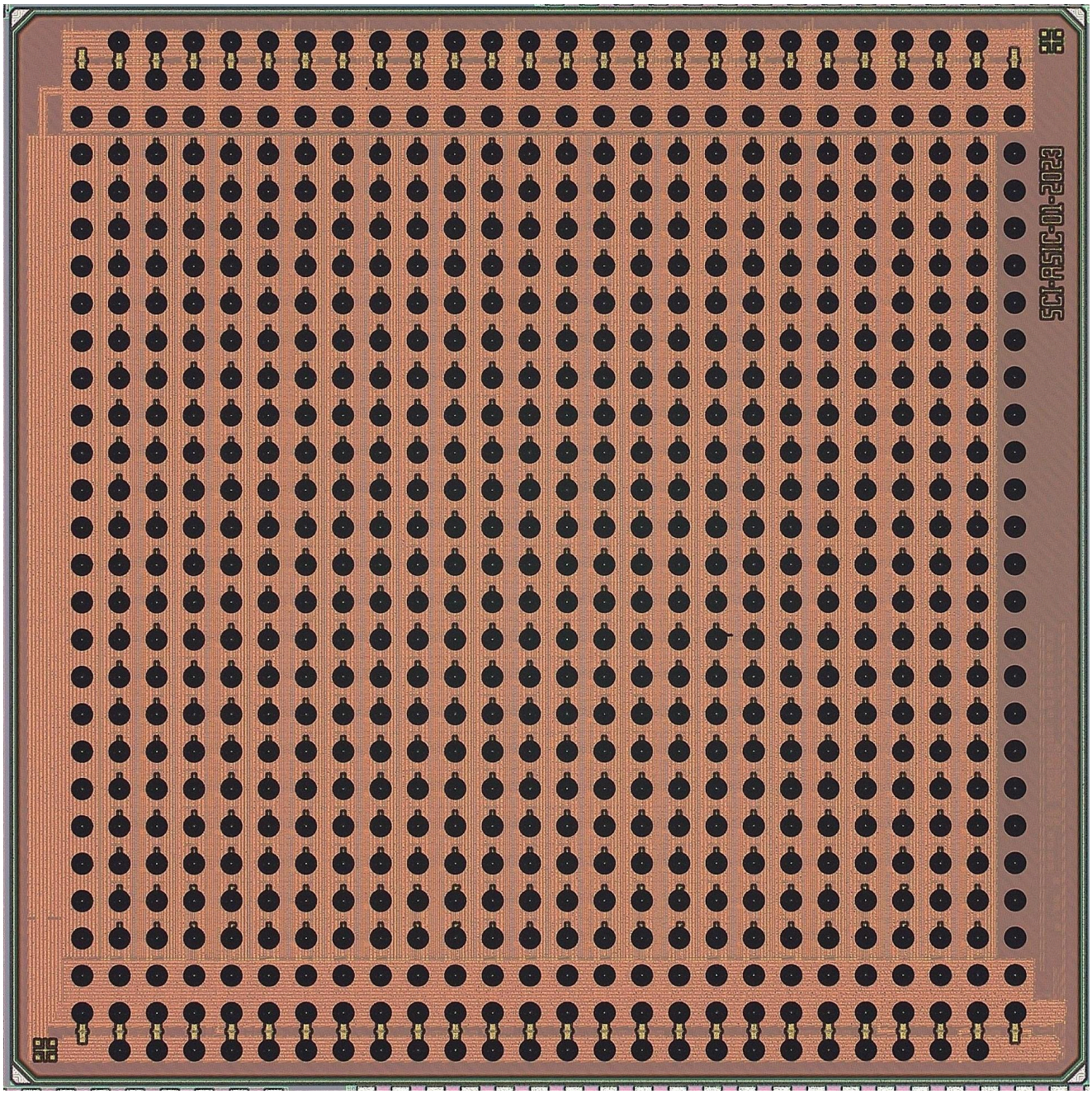
Active electrodes	Active	Reference		Test
	512	8		8
Input capacitance	6.8 pF			
Panel count	4 panels			
	One panel has 128 active electrodes, 2 reference, and 2 test electrodes			
Neural interface elements (nixels)	Selectable input configuration			
	Differential or single-ended operation			
	LNA + S/H + Comparator			
LNA parameters	Parameter name	Min		Max
	Gain, input referred noise	13 V/V, 27 µV rms		200 V/V, 4.5 µV rms
	High-pass corner	3.8 Hz		460 Hz
	Low-pass corner	1.45 kHz		14 kHz
Sample-and-hold (S/H)	Ping-pong architecture, with dual analog memory			
Comparator	In-nixel digitization with comparator Analog front-end of single-slope ADC			
ADC parameters	Single-slope-ADC, distributed architecture			
	User selectable resolution, 10–16-bit in resolution, ≤ 32 kHz in sampling			
	ADC Mode-0: *Low resolution, high sample rate*	10-bit @ 32 kHz sampling, 40 MHz clk		
	ADC Mode-1: *High resolution, mid sample rate*	12-bit @ 16 kHz sampling, 80 MHz clk		
	ADC Mode-2: *High resolution, high sample rate*	12-bit @ 32 kHz sampling, 160 MHz clk		
	ADC Mode-3: *Very high resolution low sample rate*	14-bit @ 8 kHz sampling, 160 MHz clk		
	ADC Mode-4: *Ultra high resolution very low sample rate*	16-bit @ 2kHz sampling, 160 MHz clk		
Active electrodes	Configurations	Total	Spike	LFP
	Differential, all for spike	512	480	32
	Diff. spike, single-ended LFP	496	480	16
	Single-ended spike, single-ended LFP	256	240	16
Reference electrodes	2 external reference electrodes / panel	Spike and LFP nixels have separate external reference electrode connections		
	2 external reference electrodes / chip			
	1 external reference electrodes / panel	Single external reference electrode		
	Programmable internal reference	Using internal DACs as reference		
Analog drive	On-chip bias generation	Band-gap based programmable bias generation using voltage and current mode DACs		
		12-bit v-DACs (references and test signals)		
		7-bit i-DACs		
	Ramp generation for ADC	Programmable ramp generation for ADC with variable slope and reset parameters		
Digital drive	Flexible and programmable operation of the chip	Programmable static circuit configuration of analog and digital circuits in terms of connectivity		
		Programmable timing generation for nixels and ADCs to adjust resolution and conversion time		
		Command based operation of the chip		
		Address based programming over SPI		

Programming interface	Serial	4-wire SPI
		32-bit SPI Words
		8-bit command, 8-bit address, 16-bit data
		“48 sclk cyles” per SPI operation
Test outputs	Analog	2 Analog voltage test output pads to monitor on-chip generated biases and reference voltages (pseudo-differentially)
		Voltage test outputs can be used to overwrite internally generated biases and references, including the global routing resources for reference and test electrodes used in the Nixel Array
		1 test current output to monitor on-chip generated reference and i-DAC output current
	Digital	3-bit digital test outputs to monitor internal digital signals can also be configured to work as general-purpose output pins controlled over SPI

Packaging

The Nixel 512 chip measures 4 mm x 4 mm x 0.3 mm and uses chip scale packaging with Cu bumps. The 2D bump array counts 28 rows and 26 columns with 724 total bumps (no bumps on corners) and a uniform bump pitch of 140 µm.




SCH-R512C-01-2023

Pin Specifications

Nixel 512 Chip				Center of Bump			I/O Type	Explanation	Value	Comment	Regulators	Direction	Avg. Current, Range, Resolution
Rows		Col	Bump Name	X (um)	Y0 (um)	Y1 (um)							
A	B	1	sub	240	100	240	Analog power / ground	Substrate	0.0 V				
		2	vssa_bg	380				Ground / analog / bandgap	0.0 V				
		3	vdda_bg	520				Supply / analog / bandgap	2.5 V	1.8–2.8 V adjustable	REG-1	SOURCE	≤ 5 mA (DC)
		4	vdda_lna	660				Supply / analog / LNA	2.5 V		REG-2	SOURCE	≤ 10 mA (close to DC)
		5	vssa_lna	800				Ground / analog / LNA	0.0 V				
		6	vssa_cmp	940				Ground /analog / comparator	0.0 V				
		7	vdda_cmp	1080				Supply / analog / comparator	2.5 V		REG-3	SOURCE	≤10mA (close to DC)
		8	dvdd2p5	1220				Supply / 2.5 V digital Blocks	2.5 V		REG-4	SOURCE	≤5mA (switching)
		9	dvdd	1360				Supply / digital / core + IOs	1.2 V		REG-5	SOURCE	≤ 5mA (switching)
		10	dvss	1500				Ground / digital / core + IOs	0.0 V				
		11	sub	1640				Substrate	0.0 V				
		12	vdda_lna	1780				Supply / analog / LNA	2.5 V				
		13	vssa_lna	1920				Ground / analog / LNA	0.0 V				
		14	vssa_cmp	2060				Ground /analog / comparator	0.0 V				
		15	vdda_cmp	2200				Supply / analog / comparator	2.5 V				
		16	dvdd2p5	2340				Supply / 2.5V digital blocks	2.5 V				
		17	dvdd	2480				Supply / digital / core + IOs	1.2 V				

Nixel 512 Chip				Center of Bump			I/O Type	Explanation	Value	Comment	Regulators	Direction	Avg. Current, Range, Resolution
Rows		Col	Bump Name	X (um)	Y0 (um)	Y1 (um)							
A	B	18	dvss	2620	100	240	Analog power / ground	Ground / digital / core + IOs	0.0 V				
		19	sub	2760				Substrate	0.0 V				
		20	vdda_lna	2900				Supply / analog / LNA	2.5 V				
		21	vssa_lna	3040				Ground / analog / LNA	0.0 V				
		22	vssa_cmp	3180				Ground /analog / comparator	0.0 V				
		23	vdda_cmp	3320				Supply / analog / comparator	2.5 V				
		24	itest_out	3460				Current test pad / analog / bias generator	0–32 µA sourcing (p-mirror)				
		25	vtest_out <0>	3600				Voltage test pad [0] / analog / bias generator	0–2.5 V v-DAC outputs				
		26	vtest_out <1>	3740				Voltage test pad [1] / analog / bias generator	0–2.5 V v-DAC outputs				
AG	AH	1	sub	240	3740	3880	Digital power / ground / IOs	Substrate	0.0 V				
		2	dvss	380				Ground / digital / core + IOs	0.0 V				
		3	dvdd	520				Supply / digital / core + IOs	1.2 V				
		4	csn	660				CMOS (1.2) input: SPI chip select bar	0–1.2 V	From FPGA, at negedge sclk, 50 Ω series res			
		5	sdin	800				CMOS (1.2) input: SPI data in	0–1.2V	From FPGA, at negedge sclk, 50 Ω series res			

Nixel 512 Chip				Center of Bump			I/O Type	Explanation	Value	Comment	Regulators	Direction	Avg. Current, Range, Resolution
Rows		Col	Bump Name	X (um)	Y0 (um)	Y1 (um)							
AG	AH	6	sclk	940	3740	3880	Digital power / ground / IOs	CMOS (1.2) input: SPI clock	0–1.2 V, fsclk = 1/4 fclk, ≤ 40 MHz, 50% DTC	From FPGA, at negedge sclk, 50 Ω series res			
		7	sdout	1080				CMOS (1.2) output: SPI data out	0 - 1.2 V	To FPGA, at posedge sclk, 50 Ω series res			
		8	rstb	1220				Active low asynch. reset	0 - 1.2 V	From FPGA, 50 or 20 Ω series res			
		9	clk	1360				Input: clock	0 - 1.2V, fclk ≤ 160 MHz, 50% DTC	From FPGA, 50 or 20 Ω series res			
		10	sub	1500				Substrate	0.0 V				
		11	dvss	1640				Ground / digital / core + IOs	0.0 V				
		12	dvdd	1780				Supply / digital / core + IOs	1.2 V				
		13	data_ser <0>	1920				CMOS (1.2) output: serializer data output [0]	SDR data rate, at rising edge clk, ≤ 160 Mbps	To FPGA, 50 or 20 Ω series res			
		14	wclk_ser <0>	2060				CMOS (1.2) output: serializer word clock output [0]	Frequency = 1/16 of SDR data rate	To FPGA, 50 or 20 Ω series res			

Nixel 512 Chip				Center of Bump			I/O Type	Explanation	Value	Comment	Regulators	Direction	Avg. Current, Range, Resolution
Rows		Col	Bump Name	X (um)	Y0 (um)	Y1 (um)							
AG	AH	15	data_ser <1>	2200	3740	3880	Digital power / ground / IOs	CMOS (1.2) output: serializer data output [1]	SDR data rate, at rising edge clk, ≤ 160 Mbps	To FPGA, 50 or 20 Ω series res			
		16	wclk_ser <1>	2340				CMOS (1.2) output: serializer word clock output [1]	Frequency = 1/16 of SDR data rate	To FPGA, 50 or 20 Ω series res			
		17	data_ser <2>	2480				CMOS (1.2) output: serializer data output [2]	SDR data rate, at rising edge clk, ≤ 160 Mbps	To FPGA, 50 or 20 Ω series res			
		18	wclk_ser <2>	2620				CMOS (1.2) output: serializer word clock output [2]	Frequency = 1/16 of SDR data rate	To FPGA, 50 or 20 Ω series res			
		19	data_ser <3>	2760				CMOS (1.2) output: serializer data output [3]	SDR data rate, at rising edge clk, ≤ 160 Mbps	To FPGA, 50 or 20 Ω series res			
		20	wclk_ser <3>	2900				CMOS (1.2) output: serializer word clock output [3]	Frequency = 1/16 of SDR data rate	To FPGA, 50 or 20 Ω series res			
		21	sub	3040				Substrate	0.0 V				
		22	dvss	3180				Ground / digital / core + IOs	0.0 V				
		23	dvdd	3320				Supply / digital / Core + IOs	1.2 V				

Nixel 512 Chip				Center of Bump			I/O Type	Explanation	Value	Comment	Regulators	Direction	Avg. Current, Range, Resolution
Rows		Col	Bump Name	X (um)	Y0 (um)	Y1 (um)							
AG	AH	24	digtest <0>	3460	3740	3880	Digital power / ground / IOs	CMOS (1.2) digital test output [0]	0–1.2 V	To FPGA, 50 or 20 Ω series res			
		25	digtest <1>	3600				CMOS (1.2) digital test output [1]	0–1.2 V	To FPGA, 50 or 20 Ω series res			
		26	digtest <2>	3740				CMOS (1.2) digital test output [2]	0–1.2 V	To FPGA, 50 or 20 Ω series res			

On-Chip Registers

The Nixel 512 chip contains 101 writable (RAM) registers. Below are the descriptions and default values of all of the registers.

AnaDrive

ADR	REG NAME	REG INFO / NET NAME	DEF (HEX)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	d_bgvref[7:0]	BandGap and Vref Settings	0000									test_bg[2:0]			start_bg	pd_bg	pd_ota_vref	pull_down_drv_vref	pull_up_drv_vref
1	d_irefdac[15:0]	Iref Settings	0840	pd_iref	d_iref[7:0]							d_idac[6:0]							
2	d_vdac0[12:0]	vdac0_vcm_lna	0908				pd_vdac_0	vdac_0[11:0]											
3	d_vdac1[12:0]	vdac1_vncas_lna	0908				pd_vdac_1	vdac_1[11:0]											
4	d_vdac2[12:0]	vdac2_vpcas_lna	0908				pd_vdac_2	vdac_2[11:0]											
5	d_vdac3[12:0]	vdac3_vcm_pre	0908				pd_vdac_3	vdac_2[11:0]											
6	d_vdac4[12:0]	vdac4_vref_int	073A				pd_vdac_4	vdac_4[11:0]											
7	d_vdac5[12:0]	vdac5_vref_ramp	0908				pd_vdac_5	vdac_5[11:0]											
8	d_vdac6[12:0]	vdac6_vimp	0172				pd_vdac_6	vdac_6[11:0]											
9	d_vdac7[12:0]	vdac7_vtest	0172				pd_vdac_7	vdac_7[11:0]											
10	d_vdac8[12:0]	vdac8_vref_test	0172				pd_vdac_8	vdac_8[11:0]											
11	d_vdac9[12:0]	vdac9_vncas	0908				pd_vdac_9	vdac_9[11:0]											
12	d_vdac10[12:0]	vdac10_vpcas	0908				pd_vdac_10	vdac_10[11:0]											
13	d_idac0[7:0]	idac0_vnbias_lna	0010									pd_idac_0	idac_0[6:0]						
14	d_idac1[7:0]	idac1_vpbias_pre	0010									pd_idac_1	idac_1[6:0]						
15	d_idac2[7:0]	idac2_vnbias_d2s	0010									pd_idac_2	idac_2[6:0]						
16	d_idac3[7:0]	idac3_i_int	0020									pd_idac_3	idac_3[6:0]						

AnaDrive

ADR	REG NAME	REG INFO / NET NAME	DEF (HEX)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
17	d_idac4[7:0]	idac4_ipbias_int	0020									pd_idac_4	idac_4[6:0]						
18	d_idac5[7:0]	idac5_ipbias_ramp	0020									pd_idac_5	idac_5[6:0]						
19	d_idac6[7:0]	idac6_inbias_vdac0	0050									pd_idac_6	idac_6[6:0]						
20	d_idac7[7:0]	idac7_inbias_vdac1_2	0050									pd_idac_7	idac_7[6:0]						
21	d_idac8[7:0]	idac8_inbias_vdac3	0050									pd_idac_8	idac_8[6:0]						
22	d_idac9[7:0]	idac9_inbias_vdac4	0050									pd_idac_9	idac_9[6:0]						
23	d_idac10[7:0]	idac10_inbias_vdac5	0050									pd_idac_10	idac_10[6:0]						
24	d_idac11[7:0]	idac11_inbias_vdac6_7_8	0050									pd_idac_11	idac_11[6:0]						
25	d_test[10:0]	Analog Test MUX Settings	0000						enable_itest	sel_itest	enable_vtest	sel_vtest1[3:0]				sel_vtest0[3:0]			
26	d_ramp[5:0]	RampGen Settings	0006											ramp_test_enable	ramp_pd	ramp_scap[3:0]			
27	d_eltest[15:0]	Electrode MUX Settings: Test Electrodes	0000	eltest_3[3:0]				eltest_2[3:0]				eltest_1[3:0]				eltest_0[3:0]			
28	d_elref[15:0]	Electrode MUX Settings: Ref Electrodes	CCCC	elref_3[3:0]				elref_2[3:0]				elref_1[3:0]				elref_0[3:0]			
29	d_elbus[15:0]	Electrode MUX Settings: Test Read Busses	0000	elbus_3[3:0]				elbus_2[3:0]				elbus_1[3:0]				elbus_0[3:0]			
30	d_elimp[7:0]	Electrode MUX Settings: Impedance Read Busses	0000									elimp_3[1:0]		elimp_2[1:0]		elimp_1[1:0]		elimp_0[1:0]	

Nixel

ADR	REG NAME	REG INFO	DEF (HEX)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
31	s_sw[15:0]	Nixel-BOT Input Switches	1080	spe_BOT[4:0]					sne_BOT[4:0]					simp_BOT[5:0]					
32	s_sw[31:16]	Nixel-TOP Input Switches	1080	spe_TOP[4:0]					sne_TOP[4:0]					simp_TOP[5:0]					
33	s_lna[15:0]	LNA-BOT HP + LP Filter Corner Selection	0010	lp_BOT[3:0]				hp_BOT[7:0]								gain_cap_BOT[3:0]			
34	s_lna[31:16]	LNA-TOP HP + LP Filter Corner Selection	0010	lp_TOP[3:0]				hp_TOP[7:0]								gain_cap_TOP[3:0]			
35	pd[15:0]	Power-Down for 16 Nixels, Start Index = 0	FFFF	pd[15:0]															
36	pd[31:16]	Power-Down for 16 Nixels, Start Index = 16	FFFF	pd[31:16]															
37	pd[47:32]	Power-Down for 16 Nixels, Start Index = 32	FFFF	pd[47:32]															
38	pd[63:48]	Power-Down for 16 Nixels, Start Index = 48	FFFF	pd[63:48]															
39	pd[79:64]	Power-Down for 16 Nixels, Start Index = 64	FFFF	pd[79:64]															
40	pd[95:80]	Power-Down for 16 Nixels, Start Index = 80	FFFF	pd[95:80]															
41	pd[111:96]	Power-Down for 16 Nixels, Start Index = 96	FFFF	pd[111:96]															
42	pd[127:112]	Power-Down for 16 Nixels, Start Index = 112	FFFF	pd[127:112]															
43	pd[143:128]	Power-Down for 16 Nixels, Start Index = 128	FFFF	pd[143:128]															

Nixel

ADR	REG NAME	REG INFO	DEF (HEX)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
44	pd[159:144]	Power-Down for 16 Nixels, Start Index = 144	FFFF	pd[159:144]															
45	pd[175:160]	Power-Down for 16 Nixels, Start Index = 160	FFFF	pd[175:160]															
46	pd[191:176]	Power-Down for 16 Nixels, Start Index = 176	FFFF	pd[191:176]															
47	pd[207:192]	Power-Down for 16 Nixels, Start Index = 192	FFFF	pd[207:192]															
48	pd[223:208]	Power-Down for 16 Nixels, Start Index = 208	FFFF	pd[223:208]															
49	pd[239:224]	Power-Down for 16 Nixels, Start Index = 224	FFFF	pd[239:224]															
50	pd[255:240]	Power-Down for 16 Nixels, Start Index = 240	FFFF	pd[255:240]															
51	s_cmp[15:0]	Digital Output Mux Select for Nixel	AAAA	s_cmp_3_TOP[1:0]		s_cmp_3_BOT[1:0]		s_cmp_2_TOP[1:0]		s_cmp_2_BOT[1:0]		s_cmp_1_TOP[1:0]		s_cmp_1_BOT[1:0]		s_cmp_0_TOP[1:0]		s_cmp_0_BOT[1:0]	

ADC

ADR	REG NAME	REG INFO	DEF (HEX)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
52	N_start_adc[15:0]	Start Value for ADC Counter, glb setting	00FA	N_start_ADC[15:0]															
53	N_stop_adc[15:0]	Stop Value for ADC Counters, glb setting	1324	N_stop_ADC[15:0]															
54	{gray_adc[3:0], rstb_adc[3:0]}	Gray/Bin Count Modes + ADC_Reset_Bar	0000									gray_adc[3:0]				rstb_adc[3:0]			

DigCont

ADR	REG NAME	REG INFO	DEF (HEX)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
55	sel_panel[7:0]	Panel Select for Dig. Test Outs and Ramp Controls	0011									sel_panel_test_outputs[3:0]				sel_panel_ramp_control[3:0]			
56	sel_test[14:0]	Select Active Dig. Test Outputs, 4-bit x 3 Mux Select Signals, global for all Panels	7000		enable_digtest_out[2:0]			select_digtest_out_2[3:0]				select_digtest_out_1[3:0]				select_digtest_out_0[3:0]			
57	enable_oe_ser [11:0]	Enable Serializer for Panels, ON Signal for Data /Wclk for each Panel	0FFF					enable_serializer[3:0]				enable_ wclk[3]	enable_ data[3]	enable_ wclk[2]	enable_ data[2]	enable_ wclk[1]	enable_ data[1]	enable_ wclk[0]	enable_ data[0]
58	enable_mode_ select_hs[15:0]	Enable Horizontal_Scanner, Mode Select Horizontal_Scanner	F000	enable_hs[3:0]				test_mode_select_hs_3[3:0]			test_mode_select_hs_2[3:0]	test_mode_select_hs_1[3:0]				test_mode_select_hs_0[3:0]			
59	chip_port_id_h s[15:0]	8-bit Chip ID (default h00), and 4-Port IDs for Panels. 8-bit Port IDs defauls are: 11, 10, 01, 00 (default hE4)	00E4	chip_id[7:0]								port_id_3[1:0]		port_id_2[1:0]		port_id_1[1:0]		port_id_0[1:0]	
60	spi_scan_wind ow_size[15:0]	Windowing Register for Panel-0: 8-bit Column Count, 8-bit Column Start	4000	column_count_0[7:0]								column_start_0[7:0]							
61	spi_scan_wind ow_size[31:16]	Windowing Register for Panel-1: 8-bit Column Count, 8-bit Column Start	4000	column_count_1[7:0]								column_start_1[7:0]							
62	spi_scan_wind ow_size[47:32]	Windowing Register for Panel-2: 8-bit Column Count, 8-bit Column Start	4000	column_count_2[7:0]								column_start_2[7:0]							
63	spi_scan_wind ow_size[63:48]	Windowing Register for Panel-3: 8-bit Column Count, 8-bit Column Start	4000	column_count_3[7:0]								column_start_3[7:0]							
64	spi_scan_start _time[15:0]	Horizontal Scanner Start Time for Panel-0	0032	scan_start_time_0[15:0]															

DigCont

ADR	REG NAME	REG INFO	DEF (HEX)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
65	spi_scan_start_time[31:16]	Horizontal Scanner Start Time for Panel-1	0032	scan_start_time_1[15:0]															
66	spi_scan_start_time[47:32]	Horizontal Scanner Start Time for Panel-2	0032	scan_start_time_2[15:0]															
67	spi_scan_start_time[63:48]	Horizontal Scanner Start Time for Panel-3	0032	scan_start_time_3[15:0]															
68	spi_scan_data[15:0]	SPI Scan Data: Static Test Data from SPI (for the Last MUX in Data Path, Default h2301, which is Prod ID for ASIC01	2301	spi_scan_data[15:0]															
69	enable_adc_timing_limit[7:0]	Enable for ADC Timing Generators in DigCont and Enable Count Limit for ADC Counters in DigRecord	00FF									enable_adc_timing[3:0]				enable_adc_count_limit[3:0]			
70	dtest_mode_cmp[7:0]	8-bit Mode select for D-test Signal Generation for Nixel Comps. 3-bit per Panel.	00FF									dtest_mode_cmp_3[1:0]		dtest_mode_cmp_2[1:0]		dtest_mode_cmp_1[1:0]		dtest_mode_cmp_0[1:0]	
71	dtest_data_cmp[11:0]	12-bit dtest_data from SPI Register	0000					dtest_data_cmp_3[2:0]			dtest_data_cmp_2[2:0]			dtest_data_cmp_1[2:0]			dtest_data_cmp_0[2:0]		
72	spi_direct_control[15:0]	16-bit SPI Direct Control Register for all the on-chip generated timing signals, mainly for testing purposes	0000	enable_spi_direct_control[4:0]					start_adc_direct	enable_cmp_direct	clear_cmp_direct	dtest_cmp_direct[2:0]			phi_sh_direct[2:0]			enable_ramp_direct	rst_ramp_direct
73	spi_set_rst_ramp[15:0]	Timing: SET_RST_RAMP	0032	spi_set_rst_ramp[15:0]															
74	spi_reset_rst_ramp[15:0]	Timing: RESET_RST_RAMP	012C	spi_reset_rst_ramp[15:0]															
75	spi_set_enable_ramp[15:0]	Timing: SET_ENABLE_RAMP	00FA	spi_set_enable_ramp[15:0]															

DigCont

ADR	REG NAME	REG INFO	DEF (HEX)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
76	spi_reset_enable_ramp[15:0]	Timing: RESET_ENABLE_RAMP	12F2	spi_reset_enable_ramp[15:0]															
77	spi_set_phi_sh[15:0]	Timing: SET_PHI_SH	00C8	spi_set_phi_sh[15:0]															
78	spi_reset_phi_sh[15:0]	Timing: RESET_PHI_SH	1324	spi_reset_phi_sh[15:0]															
79	spi_set_phi_rstb[15:0]	Timing: SET_PHI_RSTB	0096	spi_set_phi_rstb[15:0]															
80	spi_reset_phi_rstb[15:0]	Timing: RESET_PHI_RSTB	1356	spi_reset_phi_rstb[15:0]															
81	spi_set_dtest_cmp[15:0]	Timing: SET_DTEST_CMP	0096	spi_set_dtest_cmp[15:0]															
82	spi_reset_dtest_cmp[15:0]	Timing: RESET_DTEST_CMP	00C8	spi_reset_dtest_cmp[15:0]															
83	spi_set_clear_cmp[15:0]	Timing: SET_CLEAR_CMP	0032	spi_set_clear_cmp[15:0]															
84	spi_reset_clear_cmp[15:0]	Timing: RESET_CLEAR_CMP	0064	spi_reset_clear_cmp[15:0]															
85	spi_set_enable_cmp[15:0]	Timing: SET_ENABLE_CMP	015E	spi_set_enable_cmp[15:0]															
86	spi_reset_enable_cmp[15:0]	Timing: RESET_ENABLE_CMP	12C0	spi_reset_enable_cmp[15:0]															
87	spi_set_start_adc[15:0]	Timing: SET_START_ADC	00FA	spi_set_start_adc[15:0]															
88	spi_reset_start_adc[15:0]	Timing: RESET_START_ADC	12F2	spi_reset_start_adc[15:0]															
89	spi_line_time[15:0]	LINE TIME REGISTER for Panel-0. It is suggested to have same LINE time for all Panels.	1388	spi_line_time[15:0]															
90	spi_line_time[31:16]	LINE TIME REGISTER for Panel-1. It is suggested to have same LINE time for all Panels.	1388	spi_line_time[31:16]															

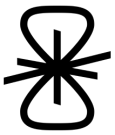
DigCont

ADR	REG NAME	REG INFO	DEF (HEX)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
91	spi_line_time[47:32]	LINE TIME REGISTER for Panel-2. It is suggested to have same LINE time for all Panels.	1388	spi_line_time[47:32]															
92	spi_line_time[63:48]	LINE TIME REGISTER for Panel-3. It is suggested to have same LINE time for all Panels.	1388	spi_line_time[63:48]															
93	{enable_line_time[3:0], auto_line_time[3:0]}	8-bit ENABLE_TRIGGER_LINE_TIME_REGISTER: Enabled all Panales by Default, Expects SPI AUTO Trigger	00F0									enable_line_time[3:0]				auto_line_time[3:0]			
94	{enable_rstb_retime[4:0], enable_signal_retime[3:0]}	9-bit ENABLE_RSTB_SIGNAL_REGISTER. All RSTB and SIGNAL Retime functions are ON by Default.	01FF								enable_rstb_retime[4:0]					enable_signal_retime[3:0]			
95	spi_gpout[2:0]	3-bit SPI_GPOUT REGISTER. Use Reg#55 to configure to use SPI_GPOUT for digtest_out[2:0]	0000														spi_gpout[2:0]		

Unused

ADR	REG NAME	REG INFO	DEF (HEX)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
96	unused_register0[15:0]	Can be used for SPI R/W Testing	0000	unused_register0[15:0]															
97	unused_register1[15:0]	Can be used for SPI R/W Testing	0000	unused_register1[15:0]															
98	unused_register2[15:0]	Can be used for SPI R/W Testing	0000	unused_register2[15:0]															
99	unused_register3[15:0]	Can be used for SPI R/W Testing	0000	unused_register3[15:0]															
100	unused_register4[15:0]	Can be used for SPI R/W Testing	0000	unused_register4[15:0]															
101	unused_register5[15:0]	Can be used for SPI R/W Testing	0000	unused_register5[15:0]															

Contact Information



Science Corporation
300 Wind River Way
Alameda, CA 94501
https://science.xyz/support/

This preliminary product datasheet may change without notice.