Pixel 16K Datasheet

128 x 128 Passive Display Driver ASIC

Product Datasheet (Version 1.0)

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Table of Contents

Summary

The Pixel 16K™ chip is a display driver IC designed for passive microLED arrays with up to 128 rows and 128 columns for a total pixel count up to 16K. It supports microLED arrays with common cathode configuration using rolling-line operation. The chip has an array of unit pixel drivers, with in-pixel digital memory, 7-bit current-mode digital-to-analog Converters (i-DACs), and high-voltage drive stage. The chip is operated using a 4-wire serial programming interface (SPI), using soft commands for all the critical timing operations in the chip, allowing flexible operation of the chip. The Pixel 16K chip has been fabricated using a high voltage CMOS process, with high (11 V), mid (5 V), and low (1.8 V) voltage devices. It measures 2.4 mm x 2.7 mm, and uses chip-scale packaging with Cu bumps.

Key Features

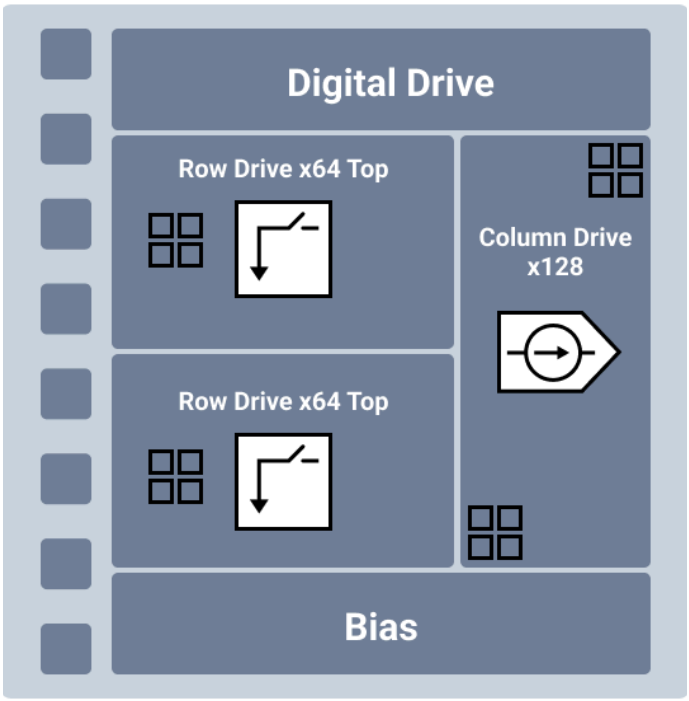
- Display driver IC for passive microLED and OLED arrays
- 128 x 128 array with common cathodes
- High-voltage current-mode pixel drivers
- In-pixel 7-bit current-mode DACs
- Pixel-level power-down control
- High voltage output drive capability up to 11 V
- Chip operated using soft commands over 4-wire SPI
- Triple supply operation
    - 11 V for high voltage output Drivers
    - 5 V analog for analog core
    - 1.8 V digital core
- Small die size of 2.7 mm x 2.4 mm
- Small chip-scale package using Cu bumps
- Suitable for flip-chip assembly

Applications

- Micro-displays using OLEDs and microLEDs
- Multi-channel current-mode DACs

Architecture

The Pixel 16K™ chip is composed of four main blocks: Row Drive, Column Drive, Bias, and Digital Drive.



The Row Drive and Column Drive are each arranged in a 2D array in the center of the chip. The Row Drive is divided into the top 64 rows and the bottom 64 rows; each composed of 64 identical unit cells arranged in an 8 x 8 array with high voltage switch arrays. Column Drivers are placed on the right of the chip, composed of 128 elements arranged in 8 x 16 format. Column Drivers contain pixel-level 7-bit current mode digital-to-analog converters (i-DACs), 8-bit pixel memory, and high voltage drive circuits. The Pixel 16K chip contains large probe pads on the right side of the chip for electrical testing and small flip-chip pads for column and row drive outputs, arranged in a 2D array on top of their corresponding drivers.

The Digital Drive controls the chip and is composed of a simple digital controller with a 4-wire SPI. The SPI controls the programming values of the pixel-level i-DACs and states of output drive transistors in the Column Drive and Row Drive using soft commands.

The Pixel 16K chip operates in rolling line scanning mode; only one row of pixels is selected and biased at a given time. First, all columns and the previously selected row are disconnected. Then, the next row is connected to ground to make the corresponding columns ready for current mode drive; the current drive levels of each column come from the previously written i-DAC values. Once the columns are connected to the anodes of the LED array, the LEDs light up during the active line time period. This cycle repeats for the other rows until the entire array has been scanned.

Each pixel has an 8-bit ping-pong type memory which allows pixel memory to be written while pixel values in the previous line time are read; this optimizes the available time and improves the scanning speed. The chip supports address-based RAM-like pixel programming to improve timing efficiency when few pixels need to be updated.

The current mode drivers in the pixels have a 4x current gain at the high voltage output stage and are driven by 5 V i-DACs. The i-DACs are biased by a global bias voltage and generated by a diode connected N-MOS transistors that are biased by a constant current provided externally through the input reference current pin (iref). For an iref of 32 µA, pixel-level i-DACs will generate current outputs between 0–127 µA in 1 µA steps. Connecting the iref to a 5 V analog supply using an adjustable resistor will generate the required input reference of 32 µA locally.

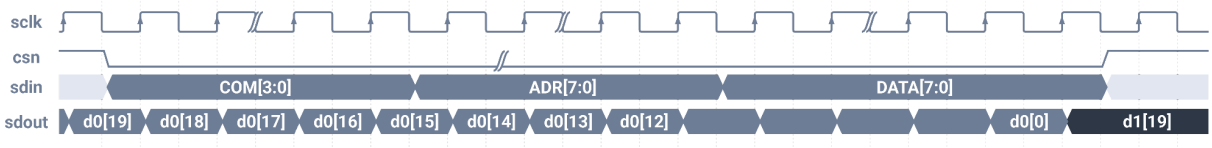
The Pixel 16K chip uses an externally provided cascode voltage (vncas_col) to isolate high voltage output devices from 5 V devices from pixel-level i-DACs.This isolation is not needed for microLED applications or other applications where high voltage supply can safely be reduced to 5 V and instead, the cascode bis voltage can safely be tied to 5 V to eliminate the generation of one external bias.

Electrical Interface

The Pixel 16K™ chip runs on triple supply voltages of 11 V for the LED drivers, 5 V for analog biasing and pixel-level i-DACs, and 1.8 V for digital control. It requires two external biases, the input reference current (iref) and the cascode voltage (vncas_col).

The Pixel 16K chip uses a standard 4-wire SPI interface to program and control the chip, with active low chip select (csn), serial data input (sdin), serial clock (sclk), and serial data output (sdout). SPI interface uses 20-bit words, composed of a 4-bit command (<19:16>), an 8-bit address (<15:8>), and an 8-bit data (<7:0>) and sends the most-significant-bit (MSB) first. Since SPI operates at the rising edge of sclk, csn and sdin are applied at the falling edge of the sclk. Likewise, sdout from the SPI will be updated at the rising edge of the sclk, therefore it should be captured by the external electronics at the falling edge of sclk.

SPI timing takes 20 sclk cycles to enter the 20-bit SPI words into the input shift register of the SPI when csn is LOW. When csn is HIGH, it takes an additional 4 sclk cycles for the SPI controller to decode the SPI commands and write to the SPI registers or execute applied soft commands. Including this idle time, an SPI operation will take at least 24 sclk cycles to complete.



The Pixel 16K chip supports sclk frequencies up to 24 MHz which corresponds to a single SPI operation of 1 µs. A single line with 128 pixels will require 128 DAC writes and approximately 12 soft commands to operate output devices individually over SPI.

When the sclk frequency is 24 MHz, the line time will take 140 µs, resulting in a frame time of 17.9 ms and a frame rate of 55.8 fps with a full resolution of 128 x 128. When half of the rows are addressed, the frame rate will double and exceed 110 fps. In that case, performance may be improved by running the Pixel 16K chip at slower sclk frequencies such as 12 MHz instead of 24 MHz.

SPI Commands

No	SPI Command Name	Short Command	Hex Code
1	No Operation	NOP	80000
2	Toggle Ping-Pong	TPP	10000
3	Write Row Address	WRA	20000
4	Disconnect Rows and Columns	DRC	30020
5	Reset Force Column	RFC	30021
6	Set Force Column	SFC	30022
7	Reset Force Row	RFR	30028
8	Connect Column Drive	CCD	3002C
9	Write Column Data	WCD	400A0

Summary Table

Power supplies and returns (grounds)	Analog power		vcc_hv	Supply for high voltage LED Drivers	11 V
			vhigh_col	Supply for column set level	10 V
			dvdd_5v	Supply for level shifters, i-DACs	5 V
	Analog ground		vss_hv	Ground for high voltage LED Drivers	0.0 V
			vlow_col	Ground for column reset level	
			dvss_5v	Ground for level shifters, i-DACs	
			sub	Substrate, ground	
	Digital power		dvdd	Supply for core logic	1.8 V
	Digital ground		dvss	Ground for core logic	0.0 V
Power dissipation	24 MHz sclk, together with LEDs	Analog	≤ 7 mW @ 10 µA drive 128 columns, 5 V vcc_hv		
		Digital	≤ 3 mW from dvdd		
		Total	≤ 10mW		
Digital I/Os	4-wire SPI		1.8 V CMOS I/Os		
			csn	Active low chip select input, generated at falling sclk	
			sdin	Serial data input, generated at falling sclk	
			sclk	Serial clk input (≤ 24 MHz, Tr=Tf ≤ 10 ns)	
			sdout	Serial data output, sampled at falling sclk, load 40 pF	
	Reset		rstb	active low reset input	
Package	Chip scale package		2.7 mm x 2.4 mm		
	Bump type		Cu bumps		
	Die thickness		12 mil (~305 µm)		

Technical Table

Product type	Display driver	Passive	
Resolution	128 x 128	16K pixels	
Design size	2.7 mm x 2.4 mm	12 mil thick (~305 µm)	
CMOS technology	130 nm high voltage CMOS	11 V, 5 V, 1.8 V active devices	
Supply voltages	High voltage	11 V and 10 V (LED Drive)	
	Mid voltage	5 V (i-DACs)	
	Low voltage	1.8 V (core logic)	
Column driver	Current mode drive	128 columns, i-DAC per column	
	DAC resolution	7-bit	
	Output drive range	0–127 µA, 1 LSB = 1 µA	
	Power-down	Per column	
Row driver	Voltage mode drive	128 Rows	
		Low and high levels	
Bias inputs	Current	iref, 32 µA into device	
	Voltage	Vncas_col, 5 V	
Digital I/Os	4-wire SPI	1.8 V CMOS	
		csn	active low chip select, generated at falling sclk
		sdin	serial data input, generated at falling sclk
		sclk	serial clk (≤ 24 MHz, Tr=Tf ≤ 10ns)
		sdout	serial data output, sampled at falling sclk, load 40 pF
I/O pad count	Wire bonding	29	Testing and probing only 60 µm x 60 µm, Pitch = 80 µm
	Flip-chip	128	Column drive
			16 rows x 8 columns
			X-pitch = 120 µm, Y-pitch = 140 µm
		128	Row drive
			16 rows x 8 columns
			X-Pitch = 120 µm, Y-Pitch = 140 µm

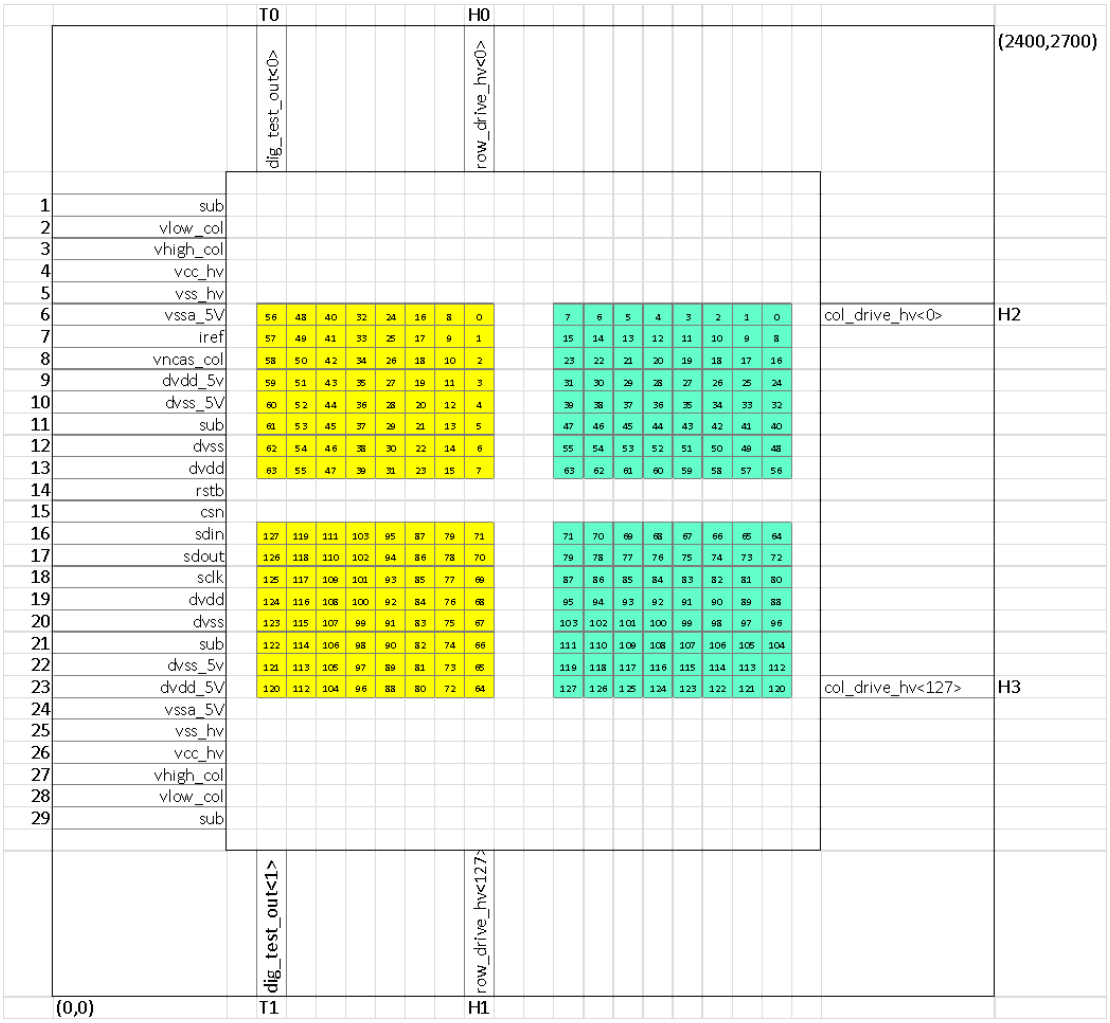
Packaging

The Pixel 16K™ chip measures 2.7 mm x 2.4 mm and uses small chip scale packaging with Cu bumps.

Bump Locations

No.	Pad Name	Location	Center of Wire Bond Pad	
			X (µm)	Y (µm)
1	sub	LEFT	50	2470
2	vlow_col	LEFT	50	2390
3	vhigh_col	LEFT	50	2310
4	vcc_hv	LEFT	50	2230
5	vss_hv	LEFT	50	2150
6	vssa_5V	LEFT	50	2070
7	iref	LEFT	50	1990
8	vncas_col	LEFT	50	1910
9	dvdd_5v	LEFT	50	1830
10	dvss_5V	LEFT	50	1750
11	sub	LEFT	50	1670
12	dvss	LEFT	50	1590
13	dvdd	LEFT	50	1510
14	rstb	LEFT	50	1430
15	csn	LEFT	50	1350
16	sdin	LEFT	50	1270
17	sdout	LEFT	50	1190
18	sclk	LEFT	50	1110
19	dvdd	LEFT	50	1030
20	dvss	LEFT	50	950
21	sub	LEFT	50	870
22	dvss_5v	LEFT	50	790
23	dvdd_5V	LEFT	50	710
24	vssa_5V	LEFT	50	630
25	vss_hv	LEFT	50	550
26	vcc_hv	LEFT	50	470
27	vhigh_col	LEFT	50	390
28	vlow_col	LEFT	50	310
29	sub	LEFT	50	230

The Row Drive and Column Drive output bumps are located in the core of the chip. The LEFT arrays are assigned to Row Drive outputs and the RIGHT arrays are assigned Column Drive outputs. The shape and locations of the Row Drive and Column Drive bumps are provided in the mechanical drawing of the Pixel 16K chip, provided under NDA.



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