Pixel A2K Datasheet

64 x 32 Passive Display Driver ASIC

Product Datasheet (Version 1.0)

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Summary

The Pixel A2K™ chip is a display driver IC designed for active microLED arrays with up to 64 columns and 32 rows for a total pixel count of 2K. It supports microLED arrays with n-type transistor unit cells and common anode LEDs. The chip uses a digital 1-bit pixel level intensity ON/OFF control programmed with a 4-wire serial programming interface (SPI); and a global analog contrast adjusted with externally provided high- and low-reference voltages used as analog gate drive voltages for the microLED arrays using a rolling update scanning method to select each pixel in a row in parallel. The chip runs at 16 MHz clock and supports a wide range of frame rates from 25 fps (40 ms frame time) up to 2500 fps (0.4 ms frame time). The Pixel A2K chip operates with a simple 4-wire SPI with an additional row timing signal. It has a miniature size of 1.33 mm x 1.33 mm, designed for flip-chip assembly using bumps.

Key Features

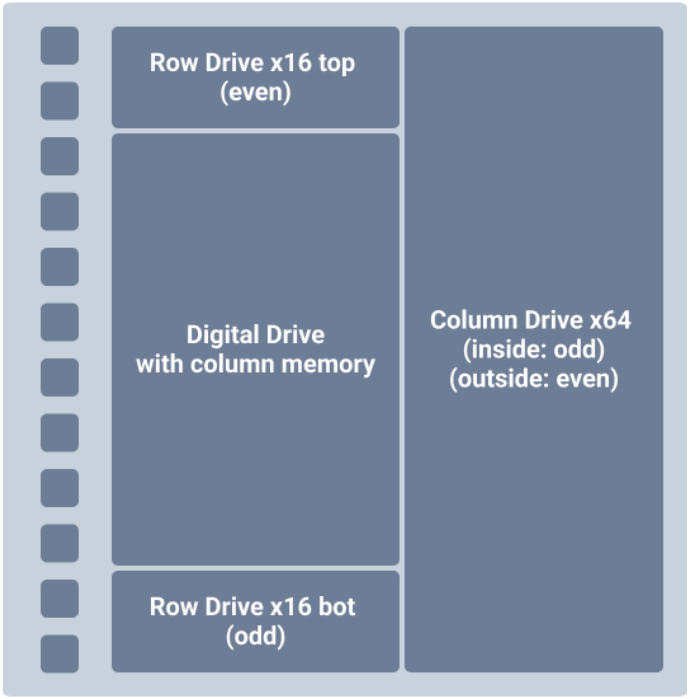
- Display driver IC for active microLED and OLED arrays
- 64 (Columns) x 32 (Rows) with common anodes
- Voltage mode bi-polar row drivers (0–5 V range)
- Global contrast control using external high / low references
- 1-bit ON/OFF intensity control for pixels
- Operates with 4-wire SPI (16 MHz clk) and 1 external row control signal
- Frame rates from 25 fps (40 ms frame time) to 2500 fps (0.4 ms frame time)
- Dual supply operation: 5 V for row and column drivers, 1.8 V for digital core
- Miniature die size of 1.33 mm x 1.33 mm
- Designed for flip-chip assembly using bumps

Applications

- MicroLED displays with ≤ 2K resolution
- Multi-channel (≤ 64) bi-polar voltage drivers with fast refresh rate (≤ 200kHz)

Architecture

The Pixel A2K™ chip is composed of three main blocks: Column Drive, Row Drive, and Digital Drive.



The column drivers are arranged in a 2 x 32 array where each unit cell in the Column Drive circuit has a 1-bit voltage mode digital analog converter (v-DAC) and column drive logic with level shifters. The v-DACs in the Column Drive circuits use externally provided high- and low-voltage references controlled by a 1-bit column ON/OFF setting stored in the column memory of the Digital Drive block to provide two level voltage drive for the active microLED arrays. The column drive logic controls the reset and voltage drive phases of the active microLED arrays. Column drivers are placed on the right of the chip with 64 driver outputs arranged in two columns using small output pads designed for flip-chip assembly.

The row drivers are placed at the top and bottom of the chip, with 16 small pads on each side. They contain row drive logic, level shifters, and 5 V CMOS drivers to control the row select transistor in the pixels of active microLED arrays. The row drive logic circuit provides a gating function using the outputs of the 32-bit row select shift register and externally applied global row timing signal. This gating function assures the write operation for analog voltages to active pixels do not overlap.

The Digital Drive controls the chip and is composed of a simple digital controller with a 4-wire SPI. The SPI uses an external global row timing signal for non-overlapping write operations of the active microLED arrays, provides soft timing commands, and holds 64-bit power-down information as ON/OFF data for the column drivers which is used for the rolling line scanning method. A logic ONE or ZERO in the serial data will correspond to OFF or ON state for the column drivers respectively. The analog data for the pixel write operation is provided by the voltage mode column drivers implemented using 1-bit v-DACs. The row-select signal required for the active pixels are provided by the row drivers implemented with 5 V CMOS logic. The

row drivers are controlled by 32-bit shift row select shift registers integrated in the Digital Drive circuit. There are two copies of the 32-bit row shift registers to select even and odd rows of the active pixel array. This allows proper timing closure in the chip and allows rolling line scanning updates in both progressive mode where rows are addressed sequentially, or in interlaced mode where even and odd rows are addressed in successive frames.

The row shift registers are operated at the falling edge of the csn signal and controlled by the soft commands captured at the rising edge of csn. Pixel values are cleared at the beginning of each write cycle to prevent any coupling between old and new pixel values. This is achieved by forcing the column driver outputs to a low voltage level defined by the OFF state of the pixels; which also helps clear the parasitic capacitors of the Column Drive nets and prepares the active pixels for a hard voltage mode reset before analog write operation.

The Pixel A2K chip uses a single external timing signal celled row to generate non-overlapping row-select signals for the active array and to prevent any coupling between successively addressed rows of the active pixel array. The write operation is started with a hard reset operation to prevent any memory effect in the pixel response. The SPI write cycle begins with the falling edge of csn signal. After some time, the row timing signal is set to HIGH, which causes the row-select signal of the selected row in the array to go HIGH and initiates the analog hard reset cycle in the voltage mode drive. During the reset cycle, csn is kept LOW to send new data to the SPI for the current row while Column Drive outputs are kept at a low reference voltage for a hard pixel reset (this will clear the analog stored voltages in the pixels). After some time, csn rises back to HIGH which causes the Column DACs to read out their most recent updated values. Once the output of the column drivers have settled, the row signal can be set to LOW to cause the row-select transistor in the active pixel to turn off and indicate the analog sampling time of the voltage outputs of the colum driver into the gate storage capacitances in the currently selected row of pixels.

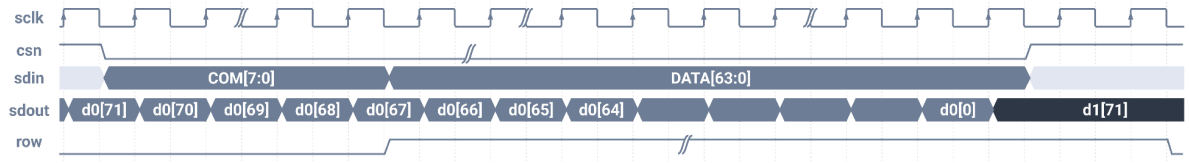
Electrical Interface

The Pixel A2K™ chip is fabricated with CMOS processes and runs on dual supply voltages of 5 V for column and row drivers and 1.8 V for digital core. The chip uses two external reference voltages (vref_low and vref_high) for the 1-bit v-DACs of the column drivers. It uses a standard 4-wire SPI interface to program and control the chip, with active low chip select (csn), serial data input (sdin), serial clock (sclk), and serial data output (sdout).

The chip measures only 1.33 mm x 1.33 mm and is designed for flip-chip packaging with small pads measuring 20 µm x 10 µm with a pitch of 30 µm. It has 12 I/O large and small pads on the left for power, ground, and digital control; 16 small pads on the top for even row drivers; 16 small pads on the bottom for odd row drivers; and 64 pads for column drivers on the right arranged into two columns. Small pads are for flip-chip assembly while large pads can be used for die probing. The large pads on the left of the chip measure 60 µm x 60 µm with an 80 µm pitch.

The Pixel A2K chip uses a standard 4-wire SPI interface to program and control the chip, with active low chip select (csn), serial data input (sdin), serial clock (sclk), and serial data output (sdout). The SPI interface uses 72-bit words composed of an 8-bit command (command<71:64>) and a 64-bit data (data<63:0>), it sends the most-significant-bit (MSB) first. Since SPI operates at the rising edge of sclk, csn and sdin are applied at the falling edge of the sclk. Likewise, sdout from the SPI will be updated at the rising edge of the sclk, therefore it should be captured by the external electronics at the falling edge of sclk.

SPI timing takes 72 sclk cycles to enter the 72-bit SPI words into the input shift register of the SPI when csn is LOW. When csn is HIGH, it takes an additional 8 sclk cycles for the SPI controller to decode the SPI commands and write to the SPI registers or execute applied soft commands. Including this idle time, an SPI operation will take at least 80 sclk cycles to complete.



The SPI write operation is practically instantaneous as it can be completed in 5 µs at a clock frequency of 16 MHz or a frame update time of 160 µs. The Pixel A2K chip can support frame rates from 2500 fps down to 25 fps, with corresponding frame times ranging from 0.4 ms up to 40 ms. For example, the ratio of available exposure time to total frame time will be 99.6% of a practical frame rate of 25 fps and only 96% when the frame rate is set to 250 fps.

Summary Table

Power supplies and returns (grounds)	High voltage power	dvdd_5v	Supply for row & column drivers		5.0 V
	Low voltage power	dvdd	Supply for digital core		1.8 V
	Ground	dvss	Ground return for supplies		0.0 V
		sub	Substrate		0.0 V
Power dissipation	60 fps, 16 MHz sclk	Analog	≤ 0.30 mW, 100 pF column load, 64 columns, 5 V operation		
		Digital	≤ 0.05 mW		
		Total	≤ 0.35 mW		
Analog inputs	vref_high	High reference voltage for v-DACs, 2.5 V ≤ vref_high ≤ 5 V			
	vref_low	Low reference voltage for v-DACs, 0 V ≤ vref_low ≤ 2.5 V			
Digital I/Os	4-wire SPI	1.8V CMOS I/Os			
		csn	Active low chip select, generated at falling sclk		
		sdin	Serial data input, generated at falling sclk		
		sclk	Serial clk (≤ 16 MHz, Tr=Tf ≤ 15 ns)		
		sdout	Serial data output, sampled at falling sclk, load 20 pF		
	External timing input	row	Provides global row timing		
Pads	Row drivers	Top	16 small pads	Even rows	For flip-chip 20 µm x 10 µm with 30 µm pitch
		Bot	16 small pads	Odd rows	
	Column drivers	Left	64 small pads	Two columns	

	CMOS I/Os	Right	12 small pads	12 x (2x3)	
			12 large pads	12 x 1	For probing 60 µm x 60 µm with 80 µm pitch
Package	Chip-scale-package	Suitable for flip-chip bonding (by default bare dies w/o bumps)			

Technical Table

Product type	Display driver	Active	
Resolution	64 x 32	2K pixels	
Design size	1.33 mm x 1.33 mm	12 mil thick (~305 µm)	
CMOS technology	180 nm high voltage CMOS	5 V and 1.8 V active devices	
Supply voltages	High voltage	5.0 V, row and column drivers	
	Low voltage	1.8 V (core logic)	
Column driver	Voltage mode driver	64 columns, v-DAC per column	
	DAC resolution	1-bit	
	High / low levels	Externally provided by *vref_low* and *vref_low*	
	Power-down	Per column	
Row driver	Voltage mode drive	32 rows, 5 V CMOS	
		Odd and even	
Reference inputs	Voltage	vref_high, high level for 1-bit v-DACs, 2.5 V ≤ vref_high ≤ 5.0 V	
		vref_low, low level for 1-bit v-DACs, 0 V ≤ vref_low ≤ 2.5 V	
Digital I/Os	4-Wire SPI	1.8 V CMOS	
		csn	Active low chip select, generated at falling sclk
		sdin	Serial data input, generated at falling sclk
		sclk	Serial clk (≤ 16 MHz, Tr=Tf ≤ 15 ns)
		sdout	Serial data output, sampled at falling sclk, load 20 pF
I/O Pad Count	Probing	12	Power and I/Os for probing only 60 µm x 60 µm, pitch = 80 µm
	Flip-chip		Power and I/Os for flip-chip 3 x 2 small pads per signal Pad size = 20 µm x 10 µm, pitch = 30 µm
		64	Column Drive
			32 rows x 2 columns
			Pad size = 20 µm x 10 µm, pitch = 30 µm
		32	Row Drive
			16 rows top and bottom
			Pad size = 20 µm x 10 µm, pitch = 30 µm
Package	Chip-scale package	Suitable for flip-chip packaging	
	Die size	1.33 mm x 1.33 mm	
	Die thickness	12 mil (~305 µm)	

Packaging

The Pixel A2K™ chip measures 1.33 mm x 1.33 mm and is designed for flip-chip assembly using bumps.

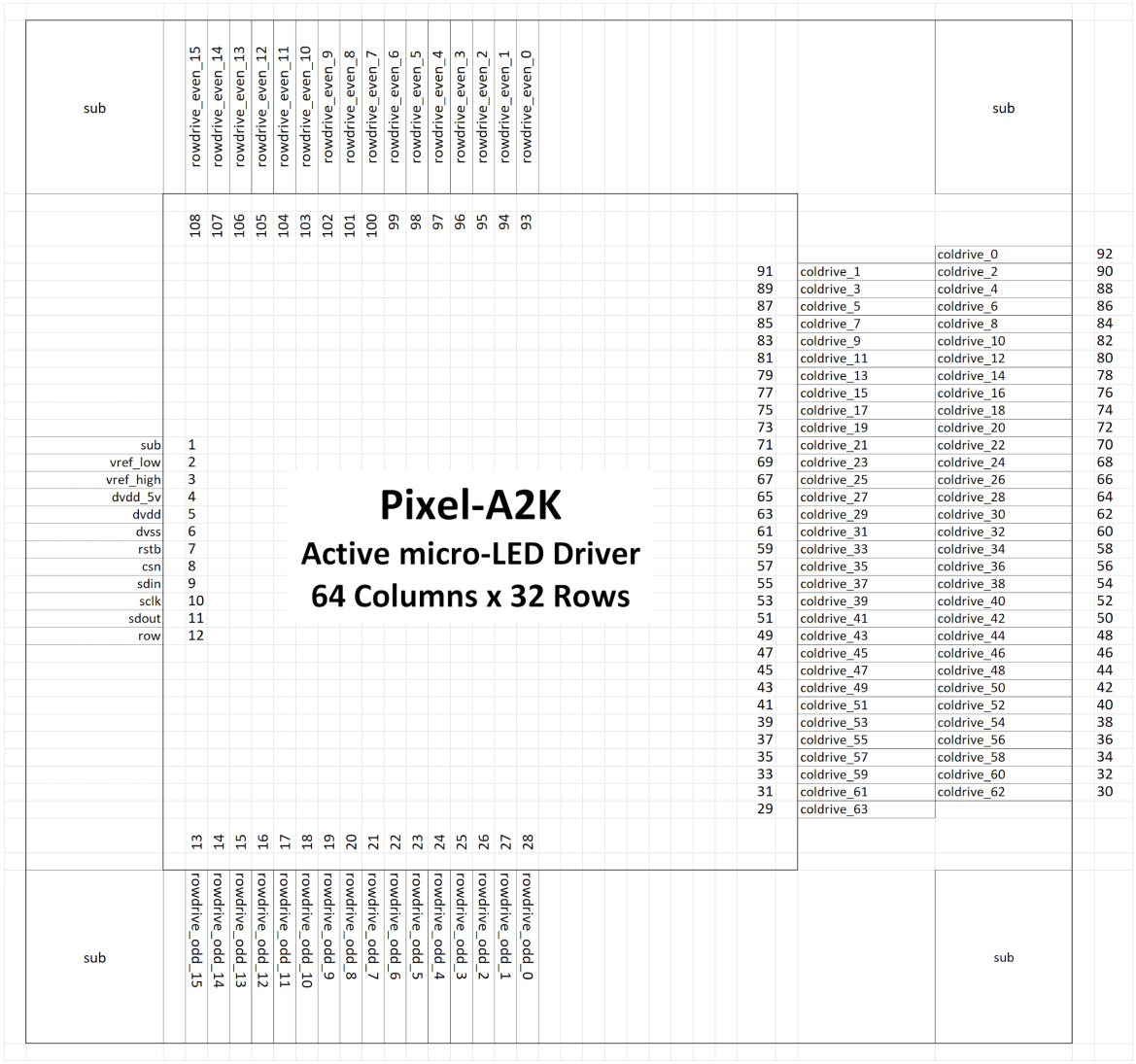
Bump Locations

Location	No	Pad Name	X (um)	Y (um)
LEFT	1	sub	47	1105
	2	vref_low		1025
	3	vref_high		945
	4	dvdd_5v		865
	5	dvdd		785
	6	dvss		705
	7	rstb		625
	8	csn		545
	9	sdin		465
	10	sclk		385
	11	sdout		305
	12	row		225
BOT	13	rowdrive_odd_15	255	27
	14	rowdrive_odd_14	285	
	15	rowdrive_odd_13	315	
	16	rowdrive_odd_12	345	
	17	rowdrive_odd_11	375	
	18	rowdrive_odd_10	405	
	19	rowdrive_odd_9	435	
	20	rowdrive_odd_8	465	
	21	rowdrive_odd_7	495	
	22	rowdrive_odd_6	525	
	23	rowdrive_odd_5	555	
	24	rowdrive_odd_4	585	
	25	rowdrive_odd_3	615	
	26	rowdrive_odd_2	645	
	27	rowdrive_odd_1	675	
	28	rowdrive_odd_0	705	
TOP	93	rowdrive_even_0	720	1303
	94	rowdrive_even_1	690	
	95	rowdrive_even_2	660	
	96	rowdrive_even_3	630	
	97	rowdrive_even_4	600	
	98	rowdrive_even_5	570	
	99	rowdrive_even_6	540	
	100	rowdrive_even_7	510	
	101	rowdrive_even_8	480	

Location	No	Pad Name	X (um)	Y (um)
TOP	102	rowdrive_even_9	450	1303
	103	rowdrive_even_10	420	
	104	rowdrive_even_11	390	
	105	rowdrive_even_12	360	
	106	rowdrive_even_13	330	
	107	rowdrive_even_14	300	
	108	rowdrive_even_15	270	
RIGHT INNER	29	coldrive_63	1263	192
	31	coldrive_61		222
	33	coldrive_59		252
	35	coldrive_57		282
	37	coldrive_55		312
	39	coldrive_53		342
	41	coldrive_51		372
	43	coldrive_49		402
	45	coldrive_47		432
	47	coldrive_45		462
	49	coldrive_43		492
	51	coldrive_41		522
	53	coldrive_39		552
	55	coldrive_37		582
	57	coldrive_35		612
	59	coldrive_33		642
	61	coldrive_31		672
	63	coldrive_29		702
	65	coldrive_27		732
	67	coldrive_25		762
	69	coldrive_23		792
	71	coldrive_21		822
	73	coldrive_19		852
	75	coldrive_17		882
	77	coldrive_15		912
	79	coldrive_13		942
	81	coldrive_11		972
	83	coldrive_9		1002
	85	coldrive_7		1032
	87	coldrive_5		1062
	89	coldrive_3		1092
	91	coldrive_1		1122
RIGHT OUTER	30	coldrive_62	1303	207
	32	coldrive_60		237
	34	coldrive_58		267
	36	coldrive_56		297
	38	coldrive_54		327
	40	coldrive_52		357
	42	coldrive_50		387
	44	coldrive_48		417
	46	coldrive_46		447

Location	No	Pad Name	X (um)	Y (um)
RIGHT OUTER	48	coldrive_44	1303	477
	50	coldrive_42		507
	52	coldrive_40		537
	54	coldrive_38		567
	56	coldrive_36		597
	58	coldrive_34		627
	60	coldrive_32		657
	62	coldrive_30		687
	64	coldrive_28		717
	66	coldrive_26		747
	68	coldrive_24		777
	70	coldrive_22		807
	72	coldrive_20		837
	74	coldrive_18		867
	76	coldrive_16		897
	78	coldrive_14		927
	80	coldrive_12		957
	82	coldrive_10		987
	84	coldrive_8		1017
	86	coldrive_6		1047
	88	coldrive_4		1077
	90	coldrive_2		1107
	92	coldrive_0		1137

Pads are located around the chip periphery with 12 power and CMOS I/O pads on the left side suitable for probing (large pads) and flip-chip bonding (small pads). There are 16 small pads on the top side for even-indexed row driver outputs and 16 small pads on the bottom side for odd-indexed row driver outputs. The column driver outputs are located on the right side of the chip arranged in two columns, odd-indexes on the inside and even-indexes on the outside. Four corner pads used for mechanical stability are connected to the substrate of the chip. The exact die dimension and locations of large and small pads used for power and CMOS I/Os and row and column drivers are provided in the mechanical drawing of the Pixel A2K chip, provided as a GDS file under NDA.



Contact Information

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